Production-Oriented Thermal Processing System and Its Processing Applications

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Abstract

Requirements for production-oriented thermal processing system are reviewed based on process variables, productivity and wafer flow in a mass production fab environment. Temperature measurement and control methods were reviewed. Direct control of wafer temperature and indirect wafer temperature control by controlling the process environment, are compared in terms of process repeatability and reliability. Effect of batch size on flexibility of system operation and productivity was discussed. Thermal processing system design approaches were introduced with a wide range of examples of thermal process applications.

Introduction

Horizontal and vertical batch furnaces have been used in thermal processing applications such as dopant diffusion, annealing, oxidation, nitridation and thermal chemical vapor deposition (CVD) since the early days of the semiconductor industry. Vertical batch furnaces are preferred in large diameter (200 and 300mm) wafer processing in terms of temperature uniformity and efficiency of usage of clean room space. Both types of batch furnaces are still widely used and able to meet the requirements for many thermal process applications.

Due to the shrinkage in device dimensions and allowable thermal budgets (more precisely, integral of diffusivity during thermal process), single wafer rapid thermal processing (RTP) systems became very popular in limited thermal processing applications. The introduction of new materials and process steps require improved ambient control. Single wafer RTP technology has significant advantages over thermal processing in traditional batch furnaces (150~200 wafers/batch) in terms of reduction of thermal budget and improved flexibility in process temperature range and lot sizes.

The processes which involve out gassing or curing often require longer heat treatment. Thick film deposition also requires longer process time. Longer process time is also beneficial to the precise thickness control of very thin film deposition. The author strongly believes that single wafer RTP and batch processing are complementary and beneficial if they are used together wisely. The author also believes that the batch size of conventional furnaces should be significantly reduced to improve operational flexibility and reduce financial risk. The wafer handling and wafer cassette storage area occupy a large portion of batch furnace floor space.

In this paper, requirements for production-oriented thermal processing systems are reviewed from the mass production point of view. Thermal processing system design approaches which address lot size flexibility and productivity requirements are introduced. .

Thermal Processing Applications

Various thermal processing applications and the process conditions used in Si wafer processing are plotted in temperature and time domain (Fig. 1). Process temperature and time are widely spread over the entire domain. Rapid thermal processes such as implant anneal and silicidation can be performed using single wafer processing systems without reducing productivity. There are still many processes which require relatively long process times which make batch furnaces attractive. In some applications, process time can be shortened by increasing process temperature so that single wafer processing is acceptable for production environments. Neither single wafer processing systems nor large batch processing systems can provide solutions to all thermal processing requirements. In practice, process conditions are often determined by a compromise between process quality and productivity of available processing systems.

To keep the process quality high and to make the process very robust, process conditions should not be compromised due to the capability of processing systems. System requirements should first be identified from the characteristics of process. Then, the system should be designed and manufactured based on the required specification to realize reasonable productivity without sacrificing process quality and repeatability.

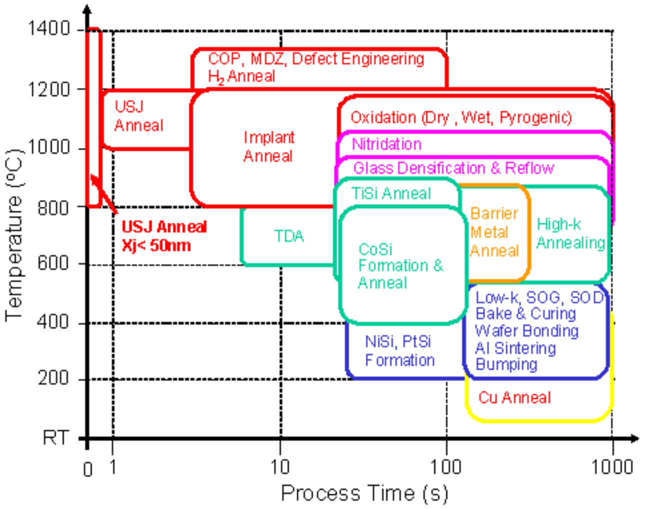

Fig. 1. Temperature-time chart of various thermal processing applications used in the semiconductor industry.

System Design Considerations

Batch Size

When wafers are processed in series using single wafer processing systems, productivity is inversely proportional to the sum of process time and overhead wafer handling time.

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Since total wafer cycle time is directly proportional to the number of wafers and the sum of process time plus overhead wafer handling time, single wafer processing is a preferred method in an R & D environment. As process time increases, productivity decreases. To overcome this problem, a multi chamber configuration is frequently adapted for production applications.

Large batch processing is a preferred method for longer processes due to its higher productivity. However, it lacks lot size flexibility and requires a significant portion of floor space for wafer and cassette handling. It is also affected by loading. On wafer uniformity, wafer-to-wafer uniformity within batch uniformity and batch-to-batch uniformity become issues depending on process applications. Dummy wafers are required in normal operation. In LPCVD applications, the process window is often determined by the pitch between wafers. To reduce cycle time and lot size flexibility, a mini-batch system which processes cassette by cassette would be a better choice compared to conventional multi-cassette processing systems.

Temperature Measurement

There are several temperature measurement techniques which are widely used in the semiconductor industry. Thermocouples are very popular to measure the temperature of objects by making a proper contact between the thermocouple and object. Proper thermocouple selection can be based on the specific temperature and atmosphere. When the direct contact between the thermocouple and wafer is a problem due to metal contamination, a ceramic or quartz sheath or cap can be used. By introducing a foreign material between the thermocouple and object, the time constant of temperature measurement will be increased. The thermocouple becomes less sensitive to the temperature change of the object. Temperature measurement using thermocouples in vacuum is very difficult due to the uncertainty in contact pressure and change in convection heat transfer characteristics.

Optical pyrometry is frequently used for measuring Si wafer temperature in lamp-based RTP systems as a non-contact temperature measurement technique. It is an effective method of estimating temperature of rotating wafers during annealing, however, it has significant drawbacks in measurement range and accuracy. The optical properties of Si must be considered when measuring or heating Si wafers by optical means. Lightly doped Si has an absorption edge near 1.2 μm and is semi-transparent in the infrared (IR) region. As the temperature increases, Si becomes less transparent and finally becomes opaque at temperatures near 600^{o}C, in the IR region. Wafer temperature measurement below 600^{o}C is not reliable using optical pyrometers. Even above 600^{o}C, the measurement is strongly influenced by the local and global optical property variations within wafer and wafer-to-wafer due to inconsistencies in dopant concentration, device patterns, backside films etc. The emissivity of Si is a function of temperature. Without knowing the local and global emissivity distribution of a wafer, it is very difficult to measure and control wafer temperature accurately. When measurement sight is blocked or the optical properties of the media, such as the window is affected (often caused by condensation or coating of materials on the window), the measured temperature value can differ from the true value. This can cause process shifts without any warning.

Temperature Control

There are two ways of controlling wafer temperature. The first one is dynamic control using in-situ wafer temperature measurement values. Typical lamp based-RTP systems employ this technique. The second one is to measure and control the process *environment* (temperature) instead of controlling wafer temperature directly. Typical furnaces fall into this category. They can also be classified as a cold wall system or hot wall system.

In a cold wall system (lamp-based RTP system), the wafer is the hottest object in the process chamber and it will naturally lose heat to the cold chamber walls. Consequently, it is very difficult to maintain temperature uniformity during the process. Temperature repeatability is also dependent on many factors such as local and global emissivity distribution on the wafer, chamber wall temperature and chamber wall reflectivity. There is a large difference in heat transfer mechanisms between single side heating and double side heating systems.

In a hot wall system (furnace-like system), a wafer is the coldest object in the process chamber at all times. As long as the process environment temperature is uniform and the thermal mass is large enough, temperature uniformity within the wafers and wafer-to-wafer temperature repeatability should not be a problem. The temperature repeatability is less dependent on local and global emissivity distribution on the wafer because uniform heat is supplied from surroundings.

Heat Source

To heat wafers uniformly, the wafer should be processed in an encapsulated isothermal process environment. A planar heat source or cavity (larger than the wafer size) with high temperature uniformity and large thermal mass would be more practical.

When an array of point heat sources with limited surface area and small thermal mass (such as tungsten halogen lamps), multi-zone power control is necessary to obtain reasonable on-wafer temperature uniformity. If heat sources with small surface area are used, the heat source temperature must be kept higher to get a specific wafer temperature. Thus, lamp-based RTP systems operate at significantly higher filament temperatures. This makes the thermal process more radiation dependent in lamp-based RTP systems compared to furnace-like systems.

Heat Transfer Mechanism

In lamp-based RTP systems, the wafer is only heated by radiation from the lamps. The joule heat generated by the lamps does not contribute to wafer heating. The wafer absorbs irradiated photon energy from the lamps. Since Si is transparent to the wavelengths in the IR region up to 600^{o}C, low temperature thermal processing using a lamp-based RTP system is not efficient or reliable. Temperature measurement error in pyrometry is significant below 600°C. Consequently, accurate temperature control is extremely difficult.

In the case of furnace-like systems, heat transfer between a heat source and an object (Si wafer) is dominated by conduction and convection at low temperatures (<800°C). As the heat source temperature becomes higher, the contribution from radiation heat transfer (exchange) in wafer heating becomes significant. In any temperature range, conduction, convection and radiation heat transfer mechanisms are fully utilized. This makes thermal processing very efficient for a wide range of temperatures, even as low as 100°C. By controlling the temperature of the environment using proper types of thermocouple(s), process temperatures can be accurately controlled from 100°C to 1150°C.

Operation Flexibility and Process Repeatability

Systems using small thermal masses as heat sources are very flexible to a change of processing temperature and are suitable for single wafer, multi-task operations which are often preferred by R & D applications. The systems usually show reasonable process repeatability. However, the system sometimes suffers poor long-term process repeatability and stability due to the difficulty in wafer temperature measurement and control and inhomogeneous degradation of heat sources. Frequent system performance checks, using monitor wafers, and frequent maintenance are required.

Systems using large thermal masses as heat sources lack flexibility in frequent operating temperature changes, however, they are superior in short-term and long-term process repeatability and stability. System maintenance and process monitoring for checking system performance are not required as frequently.

For both R & D and mass production applications, short-term and long-term process repeatability and stability (of the system) should have higher priority than wafer-to-wafer operating temperature flexibility.

Thermal Processing Systems

Three types of hot-wall-based systems has been designed for single wafer, five (5) wafer and twenty-five (25) wafer batch thermal processing to provide excellent process results without sacrificing productivity and long-term process repeatability. All the systems have heat sources with large thermal masses and provide excellent process stability. Systems can be selected based on either lot size flexibility or productivity. All systems are designed to be very compact and very energy efficient.

Single Wafer Rapid Thermal Furnace (SRTF)

For single wafer processing the process tube is made of clear quartz and has three quartz standoffs. The process tube is heated to a desired process temperature and the temperature is kept constant. A Si wafer is heated by absorbing energy from the surrounding hot walls during annealing. The process tube uses no moving parts for design simplicity and system reliability. The wafer is placed on the quartz standoffs in the middle of quartz process tube. The quartz process tube is located in a SiC cavity which acts as a heat distributor to create an isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly. The temperature of the SiC cavity is monitored and controlled at a predetermined process temperature by three embedded R-type thermocouples and the three zone heater assembly. The system is designed to operate from 200°C to 1150°C. Detailed thermal characteristics and process performance of the system have been reported elsewhere [1-3].

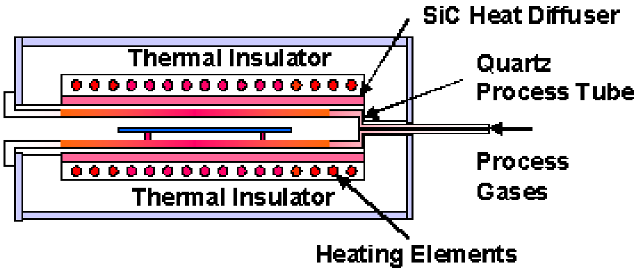


Fig. 2. Schematic illustration of single wafer process chamber.

Stacked Annealing Oven (SAO)

A hot plate-based, stacked annealing oven was designed for low temperature annealing applications in the temperature range of 100~550°C and is capable of processing five wafers simultaneously under controlled process gas environments. It was designed to provide single wafer signature, lot size flexibility and reasonable productivity with minimum facility requirements.

A side view of the stacked hot plates, with five Si wafers, is shown in Fig. 3. The design allows gradual heating of wafers for low temperature annealing and baking applications without sacrificing productivity. The individual hot plates are made of aluminum and have an embedded heater for temperature control. Aluminum was chosen as the hot plate material for temperatures up to 550°C because of its thermal stability, high thermal conductivity and ease of machining. The individual hot plates have three standoffs to accurately maintain the distance between the wafer and the hot plate surfaces. The wafers are heated by natural convection and conduction through ambient gas as well as by radiation. Hot plate temperature and process gas pressures are controlled and accurately determine the wafer temperature profile. For lower thermal conductivity gases such as N_2, O_2, Ar or air, wafer temperature rises and approaches the hot plate temperature [4]. For gases with higher thermal conductivity such as H_2, He and forming gas containing H_2 gas, the wafer temperature rises more rapidly and approaches the hot plate temperature. [4, 5]

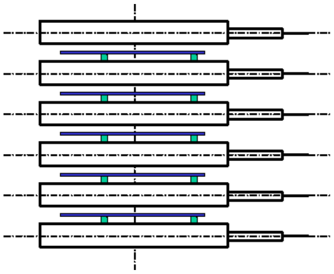


Fig. 3. Schematic illustration of a stacked hot plate system for five wafer simultaneous processing.

Mini-Batch Furnace (MBF)

Thick film growth applications by low pressure chemical vapor deposition (LPCVD) and low temperature baking and curing often takes more than ten (10) minutes at process temperature. In conventional large batch furnaces, temperature ramp-up to process temperature and temperature ramp-down from process temperature takes longer than the actual process time at process temperature due to the large thermal mass of the wafers, process tube and heating elements.

To improve cycle time and lot size flexibility, a mini-batch system which processes cassette by cassette has been designed. The mini-batch furnace can process 25 wafers at a time with a minimum (1 or 2) of dummy wafers, or without dummy wafers, depending on process applications. Unlike the large batch furnaces, the system does not require any empty cassette storage areas. As a result, the system design is very compact. By reducing the number of wafers per batch, temperature ramp-up and ramp-down speeds were shortened significantly. This feature made the cassette by cassette mini-batch furnace operation possible without decreasing productivity.

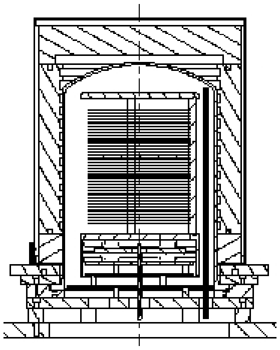


Fig. 4. Schematic illustration of mini-batch furnace for single cassette wafer processing.

Thermal Processing Applications

Thermal processing results using the SRTF, SAO and MBF systems are summarized in the temperature range of 100°C to 1150°C.

Cu Annealing (100°C~450°C)

The sheet resistance of Cu films on blanket wafers was measured before and after annealing in a forming gas atmosphere. Figure 5 shows sheet resistance reduction in 3.0 μm thick Cu films on blanket wafers as a function of annealing temperature and time. As annealing temperature and time increase, the sheet resistance was reduced drastically regardless of Cu film thickness. When the annealing temperature exceeded 200°C or the annealing time exceeded 5 min, the sheet resistance was reduced by 21~23% from the original sheet resistance. Uniformity change before or after annealing was below 1 % in 1σ.

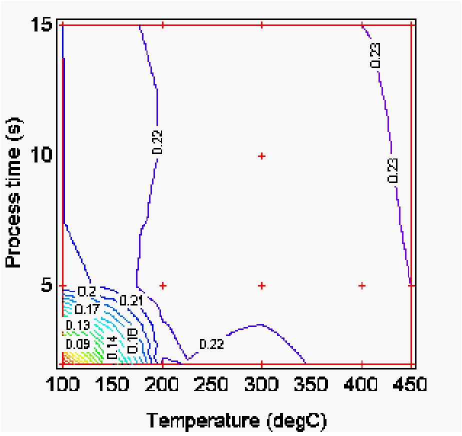


Fig. 5. Surface response of the sheet resistance reduction ratio of Cu films (3.0μm thick) as a function of annealing temperature and time.

NiSi Annealing (250°C~550°C)

Sputtered Ni films (9 nm thick) on Si wafers were annealed in the temperature range of 200~550oC to form nickel silicide. The sheet resistance of nickel silicide was measured before and after annealing. Ni_2Si formation was observed as low as 200°C. The sheet resistance was increased from 25.8 ohm/sq. to 36.0 ohm/sq. after annealing at 200°C for 5 minutes due to Ni_2Si formation. As the annealing temperature increased, the sheet resistance sharply decreased to ~10 ohm/sq. above 300°C by forming a lower resistivity NiSi phase. The uniformity change before after annealing was also below 1 % in 1σ.

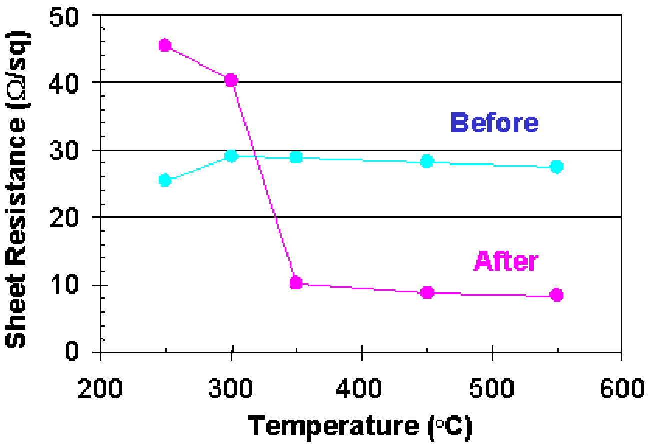


Fig. 6. Sheet resistance change of Ni films (9.0nm thick) before and after annealing at different annealing temperatures.

CoSi and TiSi Anneal (350°C ~950°C)

Silicidation anneal was performed using Co and Ti films on Si wafers in the temperature range of 350°C~950°C in an O_2-free, 100% N_2 atmosphere (1 atm) (to avoid oxidation). Figure 7 shows sheet resistance contour maps of 80nm thick Ti film on Si wafers before and after TiSi formation. The annealing condition for a TiSi formation was 600°C/60s and 800°C/60s. The uniformity change in 1σ, after wafer processing, was less than 1.0%, suggesting excellent within-wafer temperature uniformity during the process. Excellent within-wafer temperature uniformity was achieved over the entire cobalt and titanium silicidation temperature range (350°C~950°C).

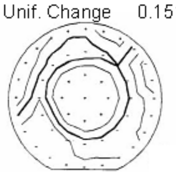
	Rs before anneal	Rs after anneal
600°C 60s	6.976 ohm/sq 1.572% 	12.854 ohm/sq 2.150% Unif. Change 0.578% 
800°C 60s	6.964 ohm/sq 1.473% 	0.953 ohm/sq 1.624% Unif. Change 0.151% 

Fig. 7. Sheet resistance contour maps of Ti layers on 200mm wafer before and after annealing. (Ti film thickness: 80nm, ambient: N_2, 760 Torr, process time: 60s)

Implant Anneal (900°C~1150°C)

Temperature sensitivity of sheet resistance of various types of deep implant wafers ($^{11}B^+$ 50keV $1x10^{15}/cm^2$, $^{49}BF_2^+$ 70keV $1x10^{15}/cm^2$, $^{31}P^+$ 70keV $1x10^{15}/cm^2$ and $^{75}As^+$ 70keV $1x10^{15}/cm^2$) was investigated in the temperature range of 900~1100°C. In all wafers, sheet resistance uniformity of less than 0.5% (1σ) was typically achieved in wide temperature and time ranges. Figure 8 shows typical sheet resistance uniformity of $^{11}B^+$ 50keV $1x10^{15}/cm^2$ and $^{49}BF_2^+$ 70keV $1x10^{15}/cm^2$ implanted wafers after annealing. Annealing was done for 35s under 1 atm N_2 atmosphere.

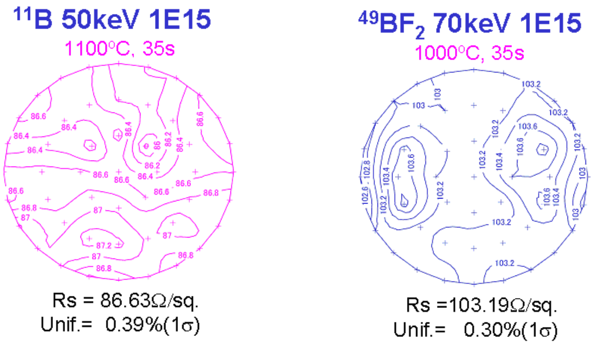


Fig. 8. Sheet resistance uniformity of $^{11}B^+$ 50keV $1x10^{15}/cm^2$ and $^{49}BF_2^+$ 70keV $1x10^{15}/cm^2$ implanted wafers after annealing.

- Dry Oxidation (900°C ~1100°C)

Thin oxide films were grown on Si wafers in the temperature range of 900~1100°C under 1 atm O_2 atmosphere. The process time was varied from 60 to 3600s while oxygen flow of 0.5 slm was maintained throughout the process. Figure 9 shows the thickness contour map of thin oxide grown for 180s. An average film thickness of 7.3nm with uniformity of 0.9% (1σ□) was obtained. No slip line was observed from oxidized wafers.

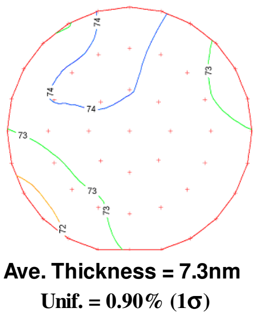


Fig. 9. Thickness uniformity of thin dry oxide (oxidation condition: 1000°C, 180s, 1atm O_2).

Other Process Applications

BPSG densification and reflow, PECVD deposited dielectric film densification, Al sintering, SOG anneal, SOD anneal have been preformed using various thermal processing systems. All the process results using these hot wall systems were equivalent or superior to those obtained from conventional large batch furnaces and/or lamp-based RTP systems. Long-term process repeatability and stability of the hot wall based systems has been proven in the mass production environment. LPCVD applications using an MBF system are being investigated.

Conclusions

System design requirements for production-oriented thermal processing systems are reviewed based on process variables, productivity and wafer flow in a mass production fab environment. Design considerations based on batch size, temperature measurement and control, heat source, heat transfer mechanisms are explained. The relationship between operation flexibility and process repeatability was discussed. A wide range of thermal process application examples using hot wall based thermal processing systems were introduced.

Acknowledgments

The author would like to thank Mr. T. Fukada, Ms. T. Murakami, Mr. I. Yokoyama, Mr. S. Fujimoto, Mr. T. Yamazaki and Mr. K. Kang of WaferMasters, Inc. for their support throughout this work. He also would like to thank Mr. J. Schram of WaferMasters, Inc. for his useful discussions and suggestions in preparation of this manuscript.

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