

# Single Wafer Rapid Thermal Furnace and Its Application to Silicidation, Oxidation and Implant Anneal

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## Biographies:

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## Abstract:

As an alternate equipment solution for energy efficient rapid thermal processing (RTP) applications, a resistively heated, vacuum and atmospheric pressure compatible, single wafer rapid thermal furnace (SRTF) system is introduced. The SRTF system is designed to provide the operational flexibility of single wafer rapid RTP systems and productivity of conventional furnaces. The design concept and hardware configuration of the SRTF system are described. The temperature measurement/control techniques and thermal characteristics of the

SRTF system are described. Process results on silicidation, oxidation and implant anneal are discussed. Sheet resistance, sheet resistance uniformity were measured in silicide wafers and implanted wafers after annealing. The secondary ion mass spectroscopy (SIMS) depth profiles were used to validate the effectiveness of implant annealing process in the SRTF system. Film thickness and thickness uniformity were also characterized in oxidized wafers.

## Data:

### - Introduction

Large batch (horizontal and vertical) furnaces have long been used in thermal processing areas including diffusion, oxidation, implant anneal etc. As demands in system operational flexibility increases and allowable thermal exposure of devices decreases, single wafer thermal processing method becomes the preferred method of processing. [1-3] The rapid thermal processing (RTP) is widely used in device manufacturing today. Two types of RTP system (lamp based single wafer RTP system and susceptor-based dual wafer RTP system) have been developed and introduced in the market. [4-5] The lamp based RTP systems have very poor energy efficiency and requires complicated temperature measurement/control algorithms. Although the susceptor based RTP systems have higher energy efficiency, their applications are limited to oxygen free environment due to the oxidation of susceptor material (SiC coated graphite) above 500°C. [5]

To overcome operational inflexibility of furnaces and poor energy efficiency of lamp based RTP systems, the authors have designed a single wafer furnace (SRTF) with a vacuum loadlock for RTP applications. In this paper, the design concept and thermal behavior of a dual chamber SRTF system

are described. Temperature repeatability, process repeatability, throughput, electric power consumption, and facility requirement were also summarized from a production point of view.

*- Single Wafer Rapid Thermal Furnace (SRTF)*

Two process chambers (furnace) are vertically stacked to maximize the usage of cleanroom space. A vacuum loadlock and two cooling stations are also vertically stacked to reduce the footprint of the system (Fig. 1). A cross-section of the SRTF is shown in Fig. 2. The process tube has three standoffs made of quartz and no moving parts inside. An R-type (Pt-13% Rh/Pt) thermocouple is embedded in one of the quartz standoffs to monitor idle process environment temperature and wafer temperature during process. During the process, a wafer is placed on the quartz standoffs (8~9mm tall) in the middle of quartz process tube. The distance between wafer and quartz walls is kept at ~10mm for both up and downward directions. The quartz process tube is located in a SiC cavity which acts as heat diffuser to create isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly.

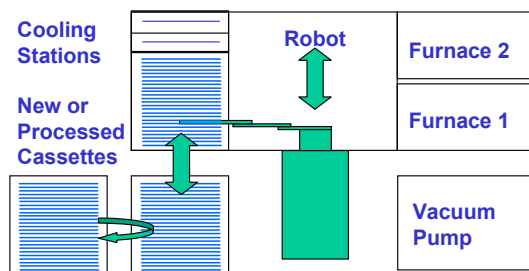


Fig. 1. Schematic illustration of stacked single wafer furnace system.

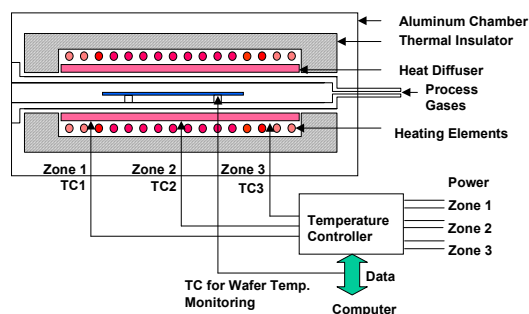


Fig. 2. Schematic diagram of individual furnace.

The entire furnace unit (quartz process tube, SiC cavity and heater assembly) is enclosed inside an aluminum chamber. In the SRTF system, the temperature of SiC cavity is monitored by three embedded R-type thermocouples and controlled by the three zone heater assembly using feedback signals from the thermocouples. The nearly identical and isothermal environment is provided to wafers regardless of wafer types and conditions. The SRTF system controls process environment (SiC cavity) temperature steady state and move wafers in and out of preheated process tube instead of controlling wafer temperature directly. The process tube employs no moving parts for durability and ease of maintenance. The system is operational under vacuum and atmospheric pressure. Since the process tube is made of quartz, the system can be used in dry/wet oxidation as well as annealing applications.

*- Ramp up and Ramp down Characteristics*

Thermal characteristics and process performance of the system are investigated in the temperature range of 200-1150°C. Wafer temperature profile during process at different SiC cavity (furnace) temperatures is monitored using a thermocouple embedded instrumentation wafer (Fig. 3). The process tube temperature is assumed to be nearly equal to the SiC cavity (furnace) temperature. The wafer temperature measurement was done under 1 atm air environment. The wafer handling sequence is as follows: (1) the wafer is introduced into furnace by a wafer handling robot, (2) the robot lowers the wafer onto the standoffs, (3) the robot leaves the furnace, (4) the wafer is kept in the furnace for the process time and (5) the robot removes the wafer from furnace at process temperature.

The wafer is naturally heated as soon as it is introduced in the preheated furnace. The wafer temperature increases rapidly and approaches the furnace temperature with time. The initial ramp rate is around 150°C/s at a furnace temperature of 1100°C. The higher the furnace temperature, the higher the initial ramp rate is. The wafer is quickly removed after processing at almost process temperature and placed into a cooling station. An exponential ramp down is observed

during natural radiation cool down. Wafer cooling is generally done in the cooling station. The wafer temperature reaches 60°C in less than 60s from wafer retrieval at 1100°C when a cooling station is used.

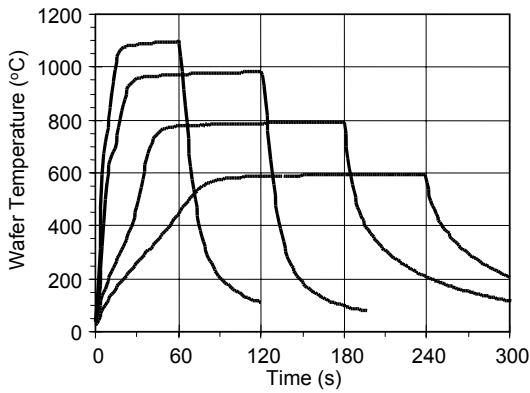


Fig. 3. Typical wafer temperature profile during process.

In lamp heated RTP system design, fast ramp-up without temperature overshooting has always been a significant technical challenge. Temperature overshooting in a SRTF system is simply not possible by nature. An excellent temperature repeatability is given as long as the SiC cavity temperature remains constant. Process time referred in lamp heated RTP system is the soak time near process temperature regardless of overhead times such as preheating, ramp-up and ramp-down times. Process time referred in the SRTF system is the wafer residence time (from wafer-in to wafer-out) in a heated furnace. The exponential ramp-up and ramp-down is considered to be ideal for preventing temperature overshooting. It is also considered to be a wafer-friendly, efficient thermal processing without increasing unnecessary process steps which result in thermal exposure increase and productivity decrease.

Since the system is vacuum/atmospheric pressure compatible and the process tube is made of quartz, a variety of process applications including annealing and oxidation are possible in the temperature range of 200-1150°C. Within wafer temperature uniformity was evaluated in terms of TiSi, implant anneal ( $^{11}\text{B}^+$ ,  $^{49}\text{BF}_2^+$ ,  $^{31}\text{P}^+$ ,  $^{75}\text{As}^+$ ) and oxidation process uniformity as well as

crystalline slip generation in the temperature range of 600~1150°C.

#### - Titanium Silicide Formation and Anneal

Temperature sensitivity of sheet resistance of TiSi and uniformity change before and after anneal are shown in Fig. 4. Ti film (35nm thick) on 200mm diameter Si (100) wafers are used. The annealing temperature was varied from 550°C to 950°C. Annealing was done for 60s under 700 Torr  $\text{N}_2$  atmosphere. The sheet resistance was measured using a four point probe. 5mm edge exclusion was used during the sheet resistance measurement. The uniformity change after process of wafers was always less than 1.0% ( $1\sigma$ ) except for phase transition regions around 580°C and 740°C. This result suggests that the within-wafer temperature uniformity during the process was excellent. The SRTF system provides excellent within-wafer temperature uniformity in the entire silicide formation and annealing temperature range.

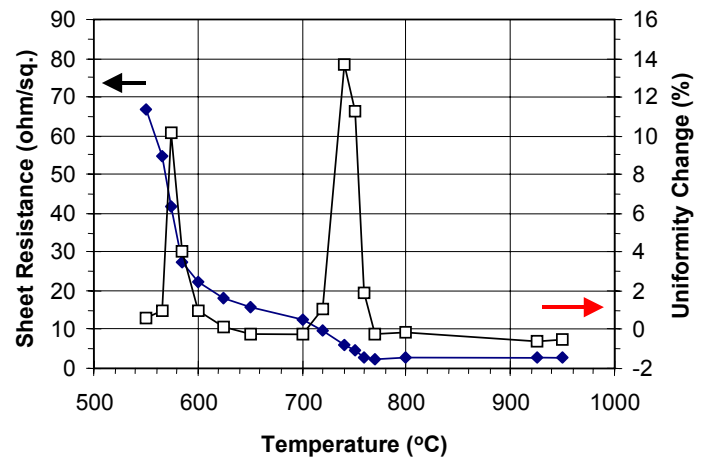


Fig. 4. Temperature sensitivity of sheet resistance of TiSi and uniformity change before and after anneal.

#### - Implant Annealing

Temperature sensitivity of sheet resistance of various types of deep implant wafers ( $^{11}\text{B}^+$  50keV  $1 \times 10^{15}/\text{cm}^2$ ,  $^{49}\text{BF}_2^+$  70keV  $1 \times 10^{15}/\text{cm}^2$ ,  $^{31}\text{P}^+$  70keV  $1 \times 10^{15}/\text{cm}^2$  and  $^{75}\text{As}^+$  70keV  $1 \times 10^{15}/\text{cm}^2$ ) was investigated in the temperature range of 900~1100°C. Annealing time (wafer residence time) was varied between 40~180s. Sheet resistance of  $^{11}\text{B}^+$  and  $^{49}\text{BF}_2^+$  implanted wafers dramatically decreases as annealing temperature

increases from 900°C to 1000°C. Above 1000°C,  $^{11}\text{B}^+$  implanted wafer continues to decrease its sheet resistance at a reduced rate while  $^{49}\text{BF}_2^+$  slightly increases its sheet resistance due to the diffusion of boron atoms during annealing. In contrast,  $^{31}\text{P}^+$  and  $^{75}\text{As}^+$  implanted wafers showed only slight decrease in their sheet resistance values even at higher temperatures. They showed very little temperature sensitivity in the temperature range of 900~1100°C.

Figure 5 shows sheet resistance uniformity of various types of implant wafers after annealing. Annealing was done in temperature range of 1000°C~1100°C. Annealing was done for 35s under 1 atm  $\text{N}_2$  atmosphere. The sheet resistance and its uniformity were comparable to or better than lamp-based RTP systems and comparable to ones obtained in conventional batch furnaces at a much faster cycle time. The process time (or cycle time) in SRTF is equivalent or better than lamp-based RTP systems and is orders of magnitude shorter than that in conventional batch furnaces.

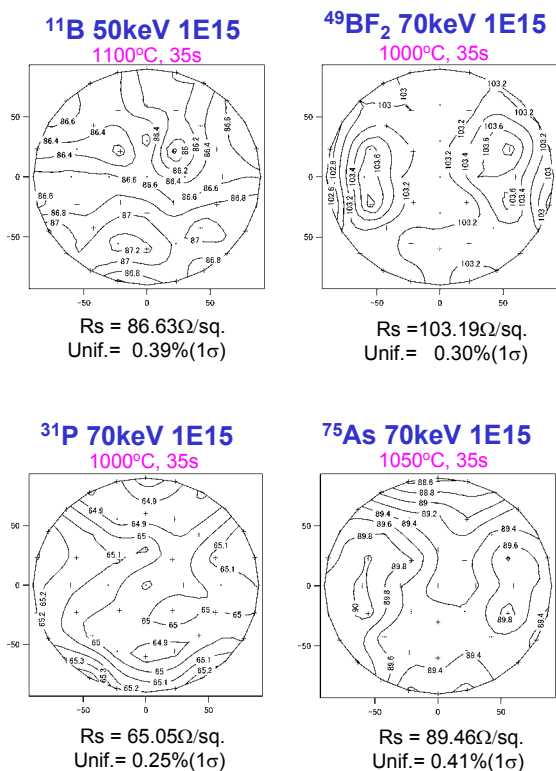


Fig. 5. Sheet resistance uniformity of implanted wafers after anneal.

### - Dry Oxidation

Thin oxide films were grown on 200mm diameter Si wafers. Dry oxidation was done at 900~1100°C under 1 atm  $\text{O}_2$  atmosphere. Process time was varied from 60 to 3600s and oxygen flow of 0.5 slm was maintained throughout the process. Figure 6 shows thickness contour map of thin oxide grown for 180s in SRTF process tube. Oxide thickness was measured by ellipsometry. 3mm edge exclusion was used for the thickness measurement. An average film thickness of 7.3nm with uniformity of 0.9% ( $1\sigma$ ) was obtained. The oxidized wafer was removed at 1000°C (oxidation temperature) under 1 atm  $\text{O}_2$  atmosphere after oxidation and placed into cooling station without changing pressure during the wafer transfer. No slip line was observed from oxidized wafers.

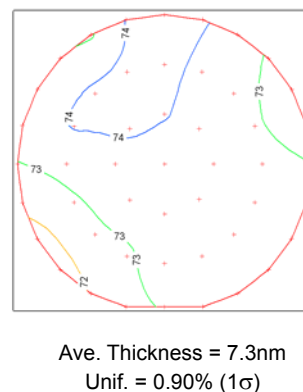


Fig. 6. Thickness contour map of thin dry oxide (oxidation condition: 1000°C, 180s, 1atm  $\text{O}_2$ ).

### Slip Free RTP Process

Defect generation including crystalline slip formation is often observed in Si wafers exposed to high temperature. Temperature nonuniformity, thermal shock and gravitational stress at high temperature can cause the crystalline slip. [6] To investigate temperature uniformity and thermal shock during high temperature process (>1000°C), bare Si wafers were annealed 1 to 10 times in the temperature range of 800~1150°C. We were able to anneal Si wafers without generating any slip lines in the temperature range of 800~1150°C by optimizing wafer transfer speed and end effector shape. X-ray topography does not indicate any slip generation in wafers processed 5 times

repeatedly in the SRTF system at 1100°C for 60s under 1 atm air after process parameter optimization. Figure 7 shows an X-ray topography photo of a wafer processed 5 times in the SRTF system at 1100°C for 60s under 1 atm air. Preliminary process results and process optimization details for slip prevention in SRTF system has been reported in previous papers. [7-8]

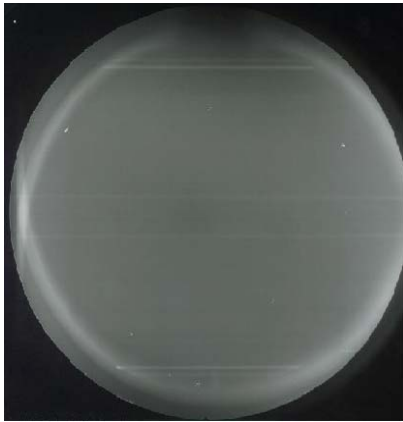


Fig. 7. X-ray topography photo of a wafer processed 5 times at 1100°C for 60s under 1 atm air.

#### *- Power Consumption and Productivity*

Photograph of the SRTF system is shown in Fig. 8. Process and slip test results obtained using the SRTF system are equivalent or better than those obtained from the conventional lamp heated RTP systems and batch furnaces. Feasibility of a new RTP system with a very simple design was demonstrated. High thermal conductivity and diffusivity of SiC cavity and optimized geometry of heater zones made this possible. Since the SRTF system has no hardware limitations affecting the length of process time, many batch furnace processes can also be done in the system with increased process flexibility and short cycle time.

Stacked dual furnace configuration of the SRTF system provides greater flexibility in process temperature. Many silicide requires two step (formation and annealing) processes at two different temperatures. [9] In the SRTF system, each process chamber can be set at different temperature. One SRTF system can handle the first (formation) step and the second (annealing)

step without waiting temperature change and stabilization from one temperature to the other.

Due to stacked dual furnace configuration and very efficient temperature ramp up/down characteristics of the SRTF system, a very high wafer throughput is achieved. Throughputs of 60~70 wafers per hour can be achieved for 60s processes with a 60s cool down step. Average steady state power consumption at 1150°C is <3.5kW per furnace. Since the SiC cavity temperature is controlled at steady state, peak power requirement does not normally exceed twice the average steady state power consumption. Lamp based RTP systems typically consume a peak power of 50~250kW per process chamber at a temperature set point of 1000°C depending on the number of lamps and lamp array. The SRTF system provides high quality process results and high process flexibility at reasonable throughput and high energy efficiency.



Fig. 8. Photograph of SRTF system for 200mm diameter wafers.

## Conclusion:

The concept and feasibility of a vacuum and atmospheric pressure compatible, stacked dual furnace SRTF system were demonstrated. Thermal characteristics and process performance of the system are investigated in detail in the temperature range of 200~1150°C. The wafer temperature profile, ramp rate, and within-wafer temperature uniformity during ramp were extensively characterized as a function of heat source temperature and process time. Excellent process performance of the SRTF system has been demonstrated in TiSi, dry oxidation and implant annealing applications in the temperature range of 200~1150°C. A very high ramp rate (~150°C/s) was obtained in the high temperature region (~1150°C) while the electric power consumption was kept minimal (<3.5kW per process chamber at 1150°C. Typical throughput for 60s process in a dual chamber is chamber system is 60~70 wph.

Many thermal processes used in furnaces and RTP systems can easily be converted to SRTF processes without decreasing cost performance and/or deteriorating process results by using the SRTF system. The power consumption of SRTF system is one or two orders of magnitude smaller than lamp-based RTP systems and conventional batch furnaces.

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