

Thermal processing in a single wafer rapid thermal furnace

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OVERVIEW

The design concept and hardware configuration of a single wafer, RTF system, plus temperature measurement/control methods and thermal characteristics are described. A production-quality process results in TiSi formation implant anneal, and thin oxide formation. Slip-free RTP results were achieved in 200mm Si wafers processed at 1100°C for 60 sec at atmospheric pressure.

Thermal processing applications such as dopant diffusion, annealing, oxidation, nitridation, and thermal chemical vapor deposition (CVD) have always been core technologies in silicon semiconductor device fabrication since the industry's inception [1]. Historically, horizontal batch furnaces were employed in the industry's early stages. To improve temperature uniformity and efficiency of cleanroom space usage, vertical batch furnaces were introduced and became very popular. Batch furnaces are able to meet the requirements for many thermal processing applications, even for 0.18 μ m technology. A typical batch furnace handles 150-200 wafers/ batch and requires long process times (4-10 hours/batch) due to slow ramp-up ($\sim 10^{\circ}\text{C}/\text{min}$) and ramp-down ($\sim 3^{\circ}\text{C}/\text{min}$) rates [2, 3].

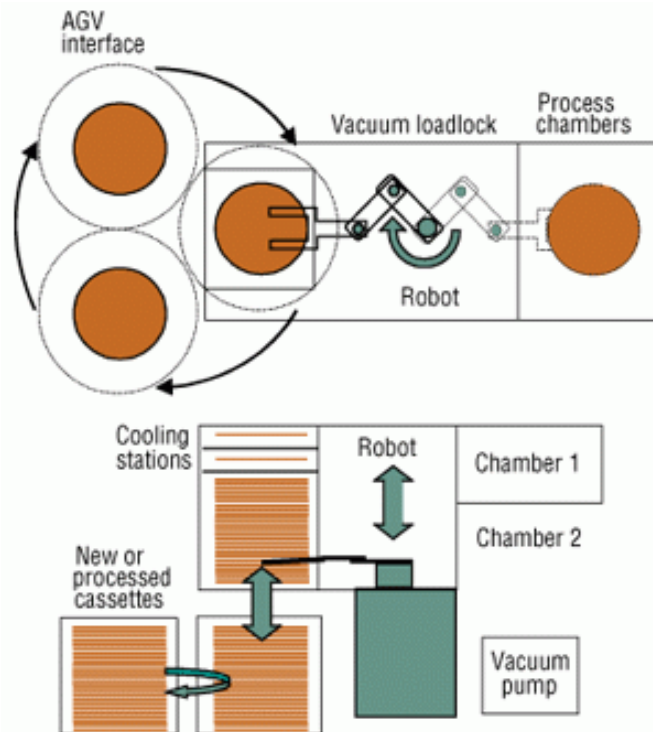


Figure 1. Schematic diagrams of a rapid thermal furnace system.

In addition to the device dimensions and allowable thermal budget decrease, the need for improved ambient control due to the introduction of new materials requires a single wafer processing system [1]. Many thermal processing applications are currently performed in single wafer, rapid thermal processing (RTP) systems. The flexibility in processing lot size, reduced cycle time and the ability for wafer-to-wafer quality control provided by single wafer processing systems has production and risk management advantages. Typical process times in the RTP system are short (1-5 min/wafer) and the ramp-up (20-250°C/sec) and ramp-down (up to 90°C/sec) rates are orders of magnitude higher than those of batch furnaces. Rapid ramp-up and ramp-down of the wafer temperature make the thermal process very efficient without increasing the thermal budget. However, the system-to-system temperature variation is relatively large [4]. Either a process parameter change or temperature calibration using process wafers is often required. A small temperature gradient on wafers heated above 1000°C can cause plastic deformation (crystalline slips), which strongly affects device yield [5, 6]. Slip-free RTP of large diameter (200mm and above) Si wafers is still a significant technical challenge.

To overcome the drawbacks of batch furnaces and single wafer RTP systems, we have designed a single wafer, rapid thermal furnace (RTF) system with a vacuum loadlock. In this paper, the design concept and thermal behavior of a vacuum-and atmospheric-pressure-compatible, dual chamber rapid thermal furnace (RTF) system are described. Wafer temperature characterization results during ramp-up and ramp-down are detailed, and temperature- dependent process results using the RTF system are presented.

Single wafer RTF

The single wafer RTF process chamber consists of a transparent quartz reactor, a silicon carbide cavity, a heater assembly, and an aluminum housing. The RTF controls the steady state temperature of the process chamber and moves wafers in and out of the preheated process chamber instead of controlling the wafer temperature directly. Two vertically stacked process chambers are attached to one side of the wafer transport module. A vacuum loadlock and two cooling stations are attached to the other side of the wafer transport module to reduce the footprint of the system. The system is also designed as an automatic guided vehicle (AGV) compatible system. (See Fig. 1.)

The furnace operates under both vacuum and atmospheric pressure conditions. Since the process chamber is made of quartz, the system can be used in normal furnace applications including oxidation and nitridation. A cross section of the RTF process chamber is shown in Fig. 2. The process chamber has three standoffs made of quartz and no moving parts inside. An R-type (Pt - 13% Rh/Pt) thermocouple is embedded in one of the quartz standoffs to monitor the idle process environment temperature and the approximate wafer temperature during process. The wafer is placed on the quartz standoffs (8-9mm tall) in the middle of the process chamber. The distance between the wafer and quartz walls is kept at ~10mm for both upward and downward directions.

The quartz process chamber is located in a SiC cavity that acts as a heat distributor to create a nearly isothermal process environment. The SiC cavity is surrounded by a three-zone heater assembly.

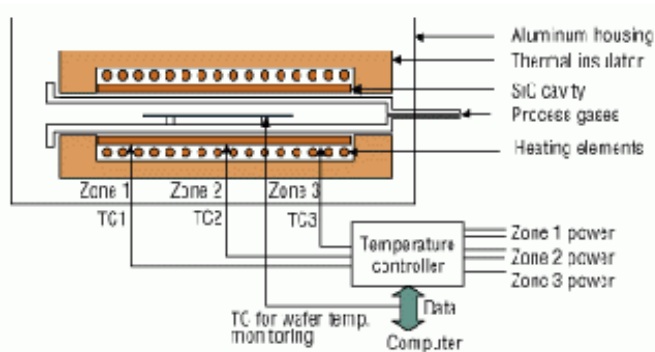


Figure 2. Cross-section illustration of a rapid thermal furnace process chamber.

The entire unit (quartz process chamber, SiC cavity, and heater assembly) is enclosed inside an aluminum chamber housing. In the RTF process chamber, the temperature of the SiC cavity is monitored by three embedded R-type thermocouples and controlled by the three-zone heater assembly using feedback signals from the thermocouples to provide identical and nearly isothermal environments to wafers regardless of wafer conditions. The process chamber temperature is kept constant at a predetermined temperature.

Wafer temperature profile during processing

The wafer temperature profile during the process at a chamber (SiC cavity) temperature of 1000°C was monitored using a thermocouple embedded instrumentation wafer (Fig. 3).

The wafer temperature measurement was done under 1atm air.

The wafer handling sequence is as follows:

1. the wafer handling robot picks up a wafer;
2. the process chamber gate valve opens;
3. the robot enters the wafer into the process chamber;
4. the robot places the wafer onto standoffs;
5. the robot leaves the process chamber;
6. the gate valve closes;
7. the wafer stays in the process chamber for a given process time;
8. the gate valve opens;
9. the robot goes into the process chamber;
10. the robot picks up the processed wafer;
11. the robot removes the wafer from the process chamber at process temperature;
12. the gate valve closes; and
13. the robot places the processed wafer into the cooling station.

As seen in Fig. 3, the wafer is heated as soon as it is introduced in the preheated process chamber. The wafer temperature increases very rapidly and approaches the process chamber temperature with time. Initial ramp rates are $\sim 100^\circ\text{C}/\text{sec}$ and $150^\circ\text{C}/\text{sec}$ at a process chamber temperature of 1100°C and 1150°C , respectively. (The relatively large difference in ramp rate with a small difference in process chamber temperature is due to the predominance of heat transfer via radiation as the temperature increases.) The wafer is

quickly removed after processing and placed into the cooling station. An exponential ramp down is observed during natural radiation cool down on the end effector. Very rapid initial ramp-down characteristics of $\sim 70^{\circ}\text{C}/\text{sec}$ and $100^{\circ}\text{C}/\text{sec}$ (for 1100°C and 1150°C chamber temperatures, respectively) are initially observed, even for the natural radiation cool-down. To enhance the wafer cooling effect below 600°C , it is generally done in the cooling station. The wafer temperature reaches 60°C in less than 60 sec from wafer retrieval at 1000°C when the cooling station is used. Figure 4 shows time-lapse wafer images during natural wafer cooling on the end effector. Wafer cooling occurred very uniformly.

Typical lamp-heated RTP systems require wafer rotation to minimize the within-wafer temperature non-uniformity due to lamp array pattern transfer during process. They also require purge, preheating, and wafer cooling steps before and after the process. To prevent slip generation during high-temperature processes, dynamic zone temperature control and slip prevention hardware such as a silicon or silicon carbide ring are employed. Fast ramp-up without temperature overshooting has always been a significant technical challenge for lamp-heated RTP system design. The process time referred to in lamp-heated RTP systems is the soak time near the process temperature regardless of overhead times such as preheating, ramp-up, and ramp-down times.

In an RTF system, temperature overshooting is not possible, and excellent temperature repeatability is given as long as the SiC cavity temperature remains constant. The process temperature and time referred to in the discussion that follow are the SiC cavity temperature and the wafer residence time (from wafer-in to wafer-out) in a heated process chamber (Fig. 3).

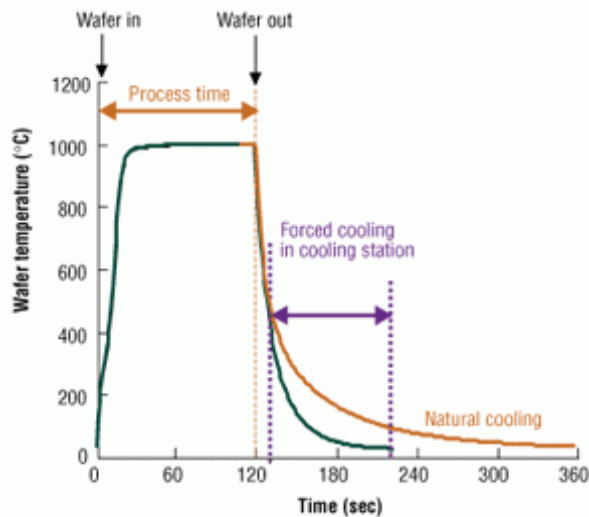


Figure 3. Wafer temperature profile and ramp rate of a 60 sec process at 1000°C .

Process and temperature uniformity

Titanium silicidation, $^{75}\text{As}^+$ implant anneal, and dry oxidation were performed to investigate process and temperature uniformity of the RTF system in its operating temperature range. Figures 5a and 5b show sheet resistance contour maps for 200mm diameter wafers after TiSi formation and anneal. The sheet resistance was measured using a four-point probe. The edge exclusion was 5mm. Ti films 80nm thick were used for testing. The annealing conditions for TiSi formation and anneal were $600^{\circ}\text{C}/60\text{ sec}$ and $800^{\circ}\text{C}/60\text{ sec}$, respectively,

under 760torr N₂ atmosphere. The 1s uniformity change after processing in both wafers was less than 1.0%.

Arsenic implant wafers with various implant energies and dosages were annealed at 800-1100°C for 35-85sec in a 760torr N₂ environment. Typical sheet resistance uniformity of implant wafers (75As+ 80keV, 1 x 10¹⁶/cm²) after annealing is shown in Fig. 5c. Annealing conditions were 915°C for 85 sec under 760torr N₂ atmosphere. The average sheet resistance and uniformity after annealing were 51.27W/sq. and 0.33% (1s), respectively.

Thin oxide films were grown by dry oxidation at 1050°C under 760torr 100% O₂ atmosphere. The process time was 60-3600 sec, and an O₂ flow of 3slm was maintained throughout the process. Figure 5d shows the thickness contour map of the thin oxide formed for 120 sec in the RTF process chamber. The oxide thickness was measured by ellipsometry. An average film thickness of 8.5nm with uniformity of 1.0% (1s) was obtained. Process results obtained using the RTF system are equivalent to or better than those obtained from the conventional lamp-heated RTP systems.

Excellent within-wafer process uniformity was achieved over the silicidation, implant anneal, and oxidation temperature range without any hardware change or process parameter modification. Excellent process uniformity suggests that the temperature within the wafer was very uniform during the process.

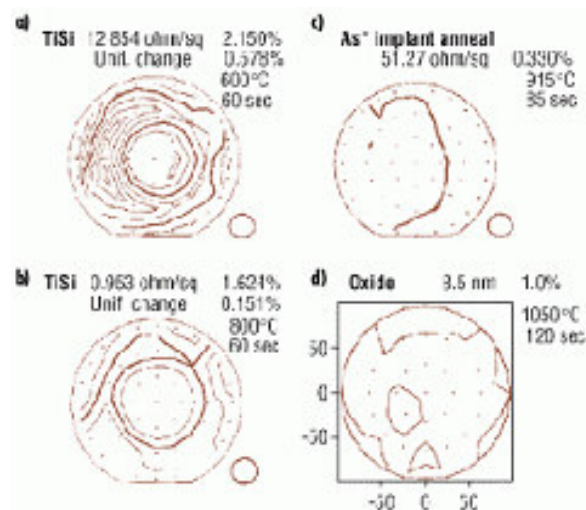


Figure 5. Typical process results. a) TiSi (600°C/60 sec, 760torr N₂); b) TiSi (800°C/60sec, 760torr N₂); c) implant anneal (75As+ 80keV, 1 x 10¹⁶/cm², 915°C/85 sec, 760torr N₂); and d) dry oxidation (1050°C/120 sec, 760torr O₂).

Slip-free high-temperature processing

To investigate the slip generation mechanism and determine a slip-free process window, 200mm bare Si (100) wafers were annealed in the temperature range of 800-1150°C for 60 sec up to 10 passes, while varying wafer transfer speed, wafer pick/place speed, wafer handling method, wafer cooling method, and other variables. Gravitational stress due to the weight of a 200mm Si wafer cannot be ignored above 1000°C if the weight is concentrated in a very small contact area [5]. Wafer cooling has to be done very uniformly to eliminate slips on the wafer edge [6]. As seen in Fig. 4, wafer cooling was done uniformly even though three small dark spots start to appear as time passes. Wafer transfer speed and wafer handling method are found to be the most important parameters to prevent slip generation during high-temperature processing.

After optimization of the wafer handling speed and method, no slip lines were observed using x-ray topography on wafers processed five times for 60 sec each in the temperature range of 800-1100°C. Six small white spots corresponding to contact points of three standoffs in the furnace and three dots on the end effector were observed in the x-ray topography image of a wafer annealed at 1100°C for 60 sec (Fig. 6). No slip lines were observed in wafers annealed five times at 1100°C for 60 sec each. This result suggests excellent within-wafer temperature uniformity and excellent gravitational stress management even at high temperatures. The authors strongly believe this high-temperature annealing technique in an RTF system can be applied to 300mm Si wafers.

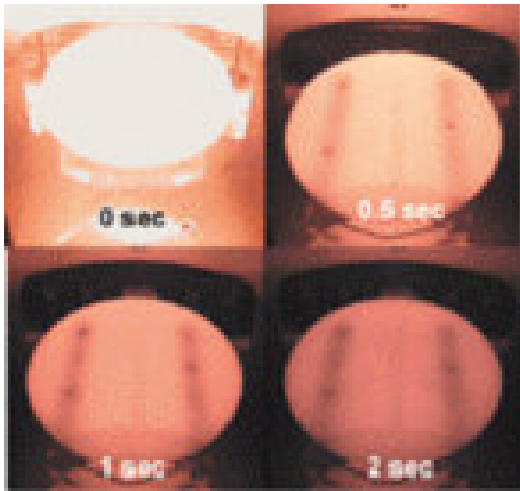


Figure 4. Time-lapse wafer images during natural wafer cooling on the end effector.



Figure 6. X-ray topography of annealed Si wafer (1100°C/60 sec, 760torr air).

Power consumption

Figure 7 shows power consumption/process chamber as a function of process chamber temperature. Average steady state power consumption at 1150°C is <3.5kW/ process chamber. Since the SiC cavity temperature is controlled at steady state, the peak power requirement does not normally exceed twice the average steady state power consumption. The power requirement in the dual chamber RTF system including a vacuum pump is less than 20kW even at 1150°C operation. In contrast, lamp-based RTP systems consume a peak power of 50-250kW/process chamber at a temperature set point of 1000°C depending on the number of lamps and lamp array.

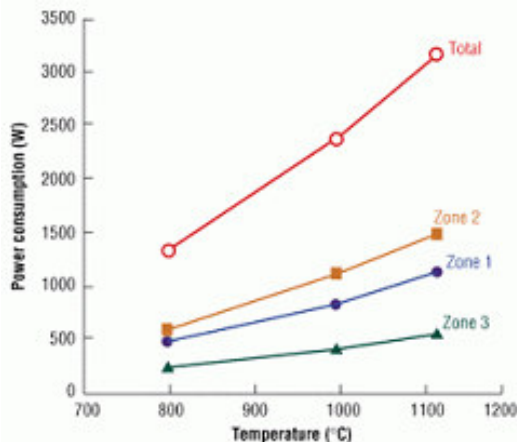


Figure 7. Power consumption of a process chamber as a function of temperature.

Productivity

The dual process chamber configuration of the RTF system provides greater flexibility in process temperature, while keeping the process chamber temperature constant. Many silicide processes require two steps (formation and annealing) at two different temperatures. In the RTF system, each process chamber can be set at a different temperature, so one system can handle the first step (formation) and the second step (annealing) without waiting for temperature change and stabilization from one temperature to the other. Due to the dual process chambers and the very efficient temperature ramp characteristics of the RTF system, a very high wafer throughput is achieved. Figure 8 shows the throughput of the RTF system as a function of process time at continuous operation with 60 sec wafer cooling under 760torr. Maximum throughput of >80 wafers/hr can be achieved for 60 sec processes when both process chambers are used. A reasonable throughput of >40 wafers/hr can be achieved even with single process chamber operation.

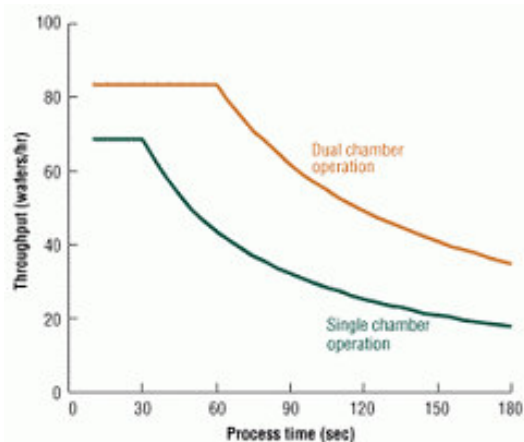


Figure 8. Throughput as a function of process time and number of process chamber used, assuming 60 sec wafer cooling and continuous processing under 760torr air.

Summary

The concept and feasibility of a vacuum-and atmospheric-pressure compatible dual chamber RTF system were demonstrated with TiSi, As+ implant anneal, and dry oxidation processes. The temperature measurement/control techniques and thermal characteristics of the RTF system were described and compared with those of conventional lamp-heated RTP systems. Repeatable slip-free RTP results were achieved in 200mm Si wafers by optimizing the wafer handling method and speed. Due to the dual process chamber configuration and steady state temperature control, a very high throughput at minimal power consumption was achieved. n

Acknowledgments

The authors would like to thank **T. Fukada, H. Kuribayashi, Y. Hiraga, D. Carman, K. Kang, and J. Lau** of WaferMasters Inc. for useful discussions and encouragement. Special thanks are due to **H. Kitayama** of Tokyo Electron Yamanashi Ltd., and **N. Takahashi and K. Sunohara** of Tokyo Electron Ltd. for their help in the project management.

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