Low Temperature Annealing System for 300mm Wafers

Woo Sik Yoo, Taro Yamazaki and Toshiyuki Uchino*
WaferMasters, Inc.
246 East Gish Road, San Jose, CA 95112 USA
*Trecenti Technologies, Inc.
751 Horiguchi, Hitachinaka, Ibaraki 312-0034, Japan

Abstract

A production worthy, five wafer annealing system using six stacked hot-plates was proposed for low temperature (100~450^{o}C) annealing applications such as Cu, Al, SOG, photo resist and low k dielectrics anneal for 300mm wafers. Thermal properties of the annealing system and wafer temperature profiles during annealing were characterized as a function of hot plate temperature and annealing time under various gas ambient. SOG process results are discussed. Productivity of the annealing system is evaluated as a function of annealing time.

1. Introduction

Traditionally, low temperature processing has been done either in a conventional large size (150~200 wafers per batch) batch furnace or on a hot plate. The conventional batch furnace provides a reasonable throughput only at a large batch processing. The hot plate system can process one wafer at a time and provides high lot size flexibility. The throughput of single wafer hot plate system decreases proportional to the process time increase. As device design advances, thermal budget becomes tighter and new materials are frequently introduced. Many of new materials such as Cu and low k dielectrics need low temperature processing. To shorten process development cycle, the development of low temperature annealing system with a improved lot size flexibility is strongly desired. In fact, the lot size flexibility is one of the important system selection criteria for 300mm wafer fabs. Single wafer processing is preferred from the view points of process quality control and production scheduling. The needs for production worthy, low cost, low temperature annealing system with processing lot size flexibility and high energy efficiency is growing rapidly as wafer size increases.

In current volume production, batch mode equipment is usually used in thermal processes. This is because single-wafer equipment had lower productivity than batch-type equipment. As a result of new equipment design concepts developed with equipment suppliers and optimized processes for single-wafer processing incorporating innovative design concepts, current single-wafer equipment has the equivalent productivity and process capability as batch systems. Currently, some critical annealing is performed by single-wafer rapid thermal processing (RTP) equipment. We presently see more and more RTP steps being used for the smaller device nodes and for virtually all 300mm wafers. One critical process parameter to enable single-wafer RTP is process time itself. Usually process time can be optimized within 1-2 minutes. However, there are processes which process time is too long for single-wafer processing. The proposed RTP system is durable for longer process time while maintaining batch type furnace advantages.

The lower thermal budget and the flexibility of single wafer processing systems makes RTP more attractive in many thermal processing applications above 600^{o}C compared to conventional batch furnaces. Most of RTP systems employ lamps for wafer heating and optical pyrometry for wafer temperature measurement and control. However, accurate and reliable wafer temperature measurement/control below 600^{o}C using optical pyrometry is still a very challenging task [1, 2]. This is because the lamp heated RTP systems use optical interaction between lamps and a Si wafer. Variation in doping level, reflective layers and/or patterns on a Si wafer has a negative influence in accurate wafer temperature measurement and control of the wafer below 600^{o}C. Moreover, highly reflective layers such as Cu film reflect more than 90% of light from lamps back to the lamps and make wafer heating difficult. [3] It also shortens the lifetime of the lamps. To reduce these problems in lamp-heated RTP systems, indirect wafer heating method is proposed for annealing wafers with highly reflective films. [3] As wafer size increases, large size batch processing becomes impractical. Significant increase in thermal mass results in the increase of temperature ramp up and ramp down time. Loading effect cannot be avoided as long as batch type systems are used. To overcome the difficulty in temperature measurement/control in RTP systems and inflexibility of conventional furnaces in lot size and turn around time, a new concept annealing systems need to be developed for low temperature annealing applications for 300mm wafers.

In this paper, a resistively heated, hot-plate based annealing system is proposed for low temperature (100~450^{o}C) annealing applications such as Cu anneal, Al anneal, SOG anneal, photoresist anneal and low k dielectrics anneal. Design concept of the annealing system is described in detail. Wafer temperature profiles during low temperature annealing in the system were characterized. SOG process results using the system are discussed. Productivity of the annealing system is evaluated as a function of annealing time.

2. System Configuration

For higher energy efficiency as well as excellent temperature uniformity, repeatability and stability, resistively heated hot plates were used as heat sources to heat 300mm Si wafers in this study. Figure 1 shows a side view and top view of stacked hot plates with a 300mm Si wafer. The hot plate is made of aluminum and has an embedded heater. Diameter and thickness of the hot plate are 400mm and 30mm, respectively. Individual hot plate has three standoffs to keep the distance between a wafer and the hot plate. The standoffs are equally spaced on the perimeter of a 210mm diameter circle. This stacked hot plate configuration was used as a heat source for wafer annealing. Loading effect which is normally observed in conventional batch processing systems can be eliminated by using stacked hot plates as heat source. Individual wafers will be surrounded by massive hot plates. In standard system configuration, six hot plates are stacked to process five 300mm wafers simultaneously.

In the operating temperature range of 100~450^{o}C, conduction and convection are the predominant heat transfer mechanisms from hot plates to a wafer. A shorter distance between hot plates provides better heat transfer to a wafer, but tolerance in wafer handling height becomes tighter. For this reason, the distance between the hot plates was kept at 20mm in this study. During annealing the wafer is places on three standoffs. The wafer will be placed approximately in the middle of two nearest hot plates. No moving parts are used in the process area. This makes system configuration simple and enhances system reliability. Wafer temperature profiles on hot plates were investigated as a function of hot plate temperature and process atmosphere.

Temperature uniformity of individual hot plates is characterized using infrared thermography in the temperature range of 100~450^{o}C. Temperature uniformity on individual hot plates is excellent. The symmetrical geometry of hot plates also helps getting excellent within hot plate temperature uniformity. The temperature variation across the hot plate is within +/- 1.0^{o}C at 400^{o}C. The excellent temperature uniformity on individual hot plates is obtained due to the high thermal conductivity of aluminum and a relatively large thickness (30mm) of hot plates. Aluminum has almost 2 times higher thermal conductivity compared to Si at room temperature. As temperature increases, the thermal conductivity ratio of Al over Si becomes larger and approaches 4 at 600K. Temperature dependence of thermal conductivity of Al, Si and air are plotted in Fig. 2. [4]

3. Wafer Temperature Profile

300mm diameter bare Si wafers with instrumentation thermocouples were annealed in the lo temperature annealing system at different temperatures under 1 atm air. The temperature of the top and bottom hot plates was controlled separately, but the temperature set points of both hot plates were kept the same. Temperature profiles of a wafer in stacked hot plates were measured at hot plate temperature set points of 200, 250, 300 and 350^{o}C under 1 atm air. The wafer handling sequence during the wafer temperature measurement is as follows: (1) the wafer handling robot picks up a wafer, (2) the robot enters the wafer between hot plates in process area, (3) the robot places the wafer onto standoffs, (4) the robot leaves the process area, (5) the wafer stays between hot plates in the process area for a given process time, (6) the robot goes into the process area, (7) the robot picks up the annealed wafer, (8) the robot removes wafer from the process area at process temperature, (9) the robot places the processed wafer into the cooling station.

Figure 3 shows wafer temperature ramp up and ramp down profiles in the system. As soon as the wafer is inserted between the stacked hot plates, the wafer temperature initially increases almost linearly and then it saturates at slightly below the hot plate temperatures. When wafer is annealed in high thermal conductivity gas ambient such as He and H_2, the wafer temperature ramp up and ramp down rate are higher than those in air. The saturated wafer temperature is also higher in He and H_2 gas ambient. The wafer temperature profiles suggest that non-contact thermal annealing method is gentle and ideal for low temperature annealing applications. [5] Multi-point wafer temperature measurements showed a very good within-wafer temperature uniformity.

4. System Configurations and Productivity

The low temperature annealing systems are configured two different ways. Figure 4 (a) and (b) show the schematic diagrams of systems. In one configuration, the stacked hot plates are exposed to the atmospheric air environment. This configuration keeps the system simple in structure and provides high productivity. The atmospheric system consists of two FOUP openers, an atmospheric wafer handling robot, six hot plates and five cooling stations. Applications such as SOG anneal, photoresist bake can be done in this type of system. Simultaneous five wafer processing is done in the system without the loading effect. Productivity of the system is not much affected by annealing time up to 5 min because of the five wafer simultaneous processing. The other configuration is designed for applications which have to be done in oxygen free ambient. In the air tight (oxygen free) system, a loadlock (also serves as cooling stations), transport module (including a vacuum wafer handling robot) and the stacked hot plates are surrounded by an aluminum enclosure. The system also has two FOUP openers and an atmospheric wafer handling robot. This system is designed for low temperature annealing processes in controlled gas environment such as H_2 mixture environment. To maximize productivity and process gas efficiency, 25 wafers are loaded into the loadlock prior to the process start. This configuration also allows five wafer simultaneous processing.

Figure 5 shows the throughput as a function of annealing time in the atmospheric annealing system and the air tight annealing system. For 1 to 3 min annealing processes, the wafer handling is the limiting factor and the throughput is ~60 wph. For annealing processes over 4 min, the annealing time is the limiting factor for throughput. For 4 and 5 min annealing processes, we were able to achieve approximately 50 and 40 wph, respectively. Due to the five-wafer simultaneous processing capability and gentle wafer temperature ramp up characteristics of the system, we are able to achieve very repeatable process results at higher productivity compared to conventional single hot plates and batch furnaces. Lot size flexibility is also improved compared to the batch furnaces without deteriorating productivity. Typical throughput of the air tight annealing system is around 20 wph for 5 min process. Power consumption of both atmospheric annealing system and the air tight annealing system is between 3~7kW at maximum process temperature of 450^{o}C.

5. SOG Anneal and Other Applications

SOG involves spin coating and annealing (baking and curing). Several low temperature (up to 400^{o}C) thermal treatments are necessary to ensure that the desired thickness and physical property are obtained and the solvents are removed from the SOG. Control of the thermal treatment of SOG films is very important for SOG processing in general. Insufficient curing will cause moisture and solvent outgassing through the vias during the subsequent metal deposition, which is known as “poisoned vias.”

During the SOG baking and curing process, the solvents and water outgas from the film. This causes considerable volume shrinkage in the SOG and creates a high tensile stress in the film. This stress could cause cracking in the SOG. Improper baking and curing very quickly could cause the upper layers of the SOG to be completely polymerized and prevent adequate moisture and/or solvent evaporation from the bulk of the SOG. Outgassing can cause trapping of hot and volatile compounds under a cap of fully polymerized SOG at the upper layer of the SOG. These trapped volatile compounds may also then contribute to cracking and popping. [6-8] To provide sufficient time for outgassing of the solvents and moisture, the baking and curing must be performed without causing any thermal shock. [6] Thermal shock at SOG bake and cure must be reduced. A gradual increase in temperature is considered to be ideal for baking and curing cycle. The SOG is typically baked on hot plates and cured in batch furnaces. Thermal shock during the hot plate baking makes the process control difficult. A long time gradual heating in a single wafer annealing system is not practical from the view point of productivity. A long process cycle and large batch size processing poses cueing problem for small size production lots. Large batch processing in a furnace often causes particle problem due to the high concentration of solvents and water vapor released from SOG films.

Spin-coated organic SOG films on 200mm wafers were baked in the five-wafer atmospheric annealing system under 1 atm air. An average as-spun thickness and refractive index of SOG films were 360 nm and 1.428, respectively. The annealing temperature was varied from 200°C to 400°C. The annealing time was also varied between 1 and 5 min. The annealing temperature and time referred to in this paper are the hot plate temperature and the wafer residence time (from wafer-in to wafer-out) between the stacked hot plates. The film thickness shrinkage and refractive index change after annealing under different conditions were plotted in Figs. 6 (a) ~ (d). As annealing temperature and time increase, thickness shrinks more due to the loss of solvents and water from the SOG film. Thickness shrinkage was controlled between 3 and 20% by adjusting an annealing temperature and time. The target thickness of SOG films after annealing is 300 nm. The thickness shrinkage of 17~20% and refractive index of 1.420 are desired for preventing cracking during annealing (baking) and obtaining desirable selectivity of etch rate in the following etch back process step. The refractive index of films also decreases with the annealing temperature and time increase.

The refractive index and average thickness shrinkage of SOG films were measured before and after annealing. The refractive index of SOG films shows very strong correlation with the average thickness shrinkage of SOG films regardless of annealing temperature and time. The refractive index decreases as the SOG film shrinks. It decreases gradually up to 18% of thickness shrinkage and drops abruptly beyond 18% of thickness shrinkage. Average thickness uniformity of SOG films after annealing ranges from 0.5 to 1.5% (1σ). The desired thickness of 300 nm (equivalent to thickness shrinkage of 17~20%) and refractive index of 1.420 can be obtained by selecting appropriate annealing temperature and time. It is possible to control SOG film shrinkage and properties using the atmospheric annealing system in the wide range of process conditions. [9] The repeatability in thickness shrinkage, refractive index and etch rate selectivity of SOG films after annealing were investigated using device production wafers. Split device yield tests were done between conventional batch furnace, conventional contact-type hot plate and the atmospheric low temperature annealing system. The atmospheric low temperature annealing system provided the highest device yield. Device test results on 200mm production wafers indicate excellent reliability and repeatability of the SOG annealing process in the atmospheric annealing system.

In the air-tight system describe in the previous section, Al sintering process and passivation process were successfully performed in the pilot production environment. Both atmospheric system and air-tight stacked hot-plate based annealing system is very promising for low temperature annealing processes such as Cu anneal, photoresist baking and low k dielectrics annealing applications. The system concept can also be applied for low temperature annealing processes for compound semiconductor wafers such as GaAs and InP.

6. Summary

A production worthy, five-wafer annealing oven using six stacked hot-plates was proposed for low temperature (100~450°C) annealing applications for 300mm wafers. Thermal properties of the annealing system using the stacked hot plates and wafer temperature profiles during annealing were characterized as a function of hot plate temperature and annealing time under various gas ambient. Two types of system configuration were introduced. Productivity of the annealing system is evaluated as a function of annealing time. SOG films were annealed in the stacked annealing oven under various annealing conditions. Change in physical properties of SOG films before and after anneal was characterized as a function of annealing temperature and time. The amount of film shrinkage and the refractive index of SOG films were controlled by selecting annealing conditions. Productivity and lot size flexibility in the five-wafer atmospheric annealing system were significantly improved compared to conventional SOG annealing methods using hot plates and batch furnaces. Uniform and repeatable SOG annealing results are achieved in the five-wafer atmospheric annealing system. The low temperature annealing system which employs stacked hot plates is also very promising for low temperature annealing processes such as Cu anneal, Al anneal, photoresist baking and low k dielectrics annealing applications.

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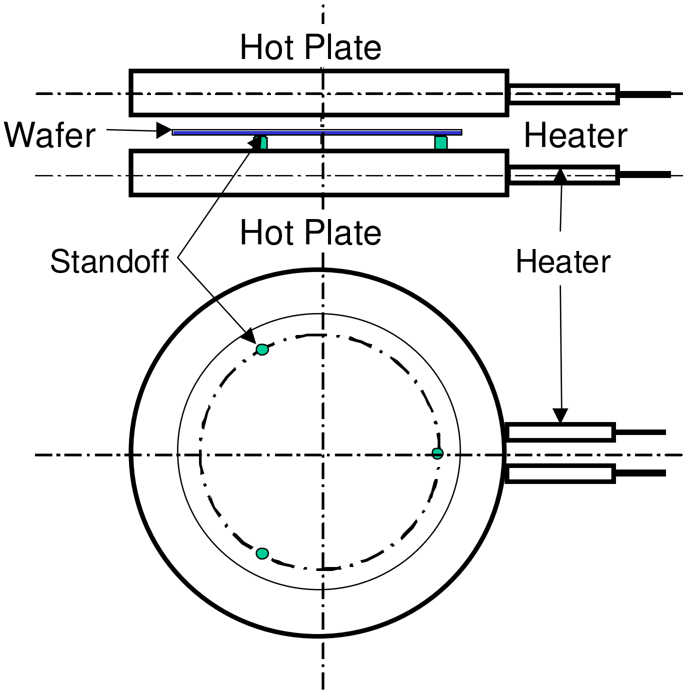


Fig. 1 Schematic diagram of a 300mm Si wafer between stacked hot plates.

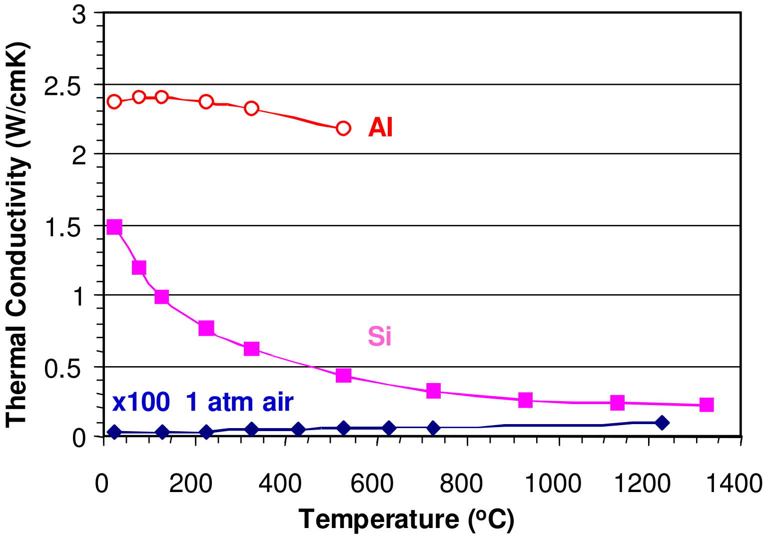


Fig. 2 Temperature dependence of thermal conductivity of Al, Si and air.

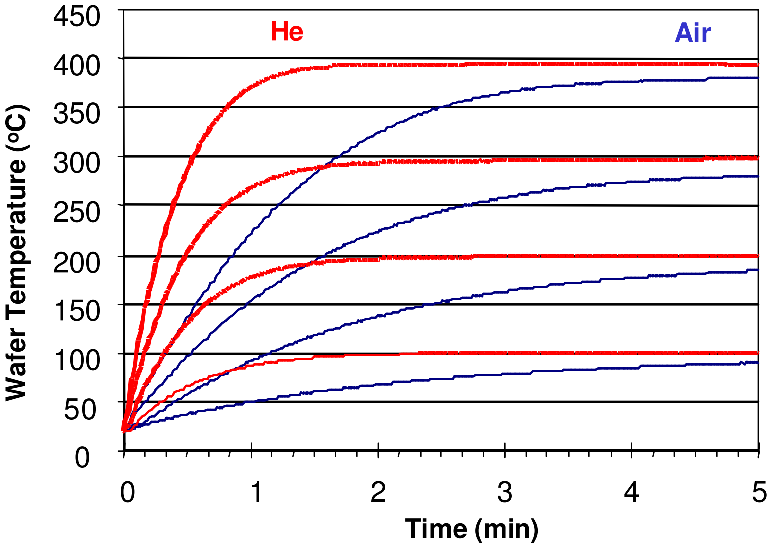
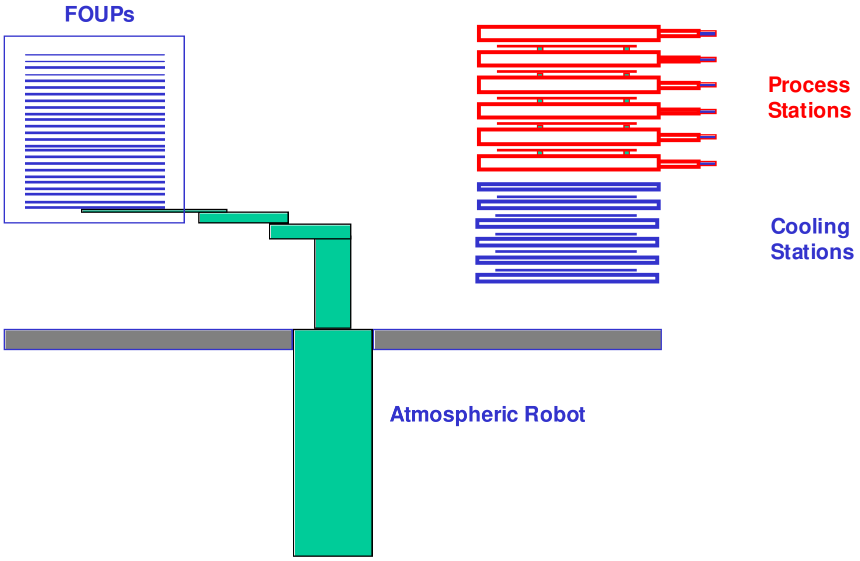


Fig. 3 Wafer temperature ramp rate at different hot plate temperatures under He and air environment.



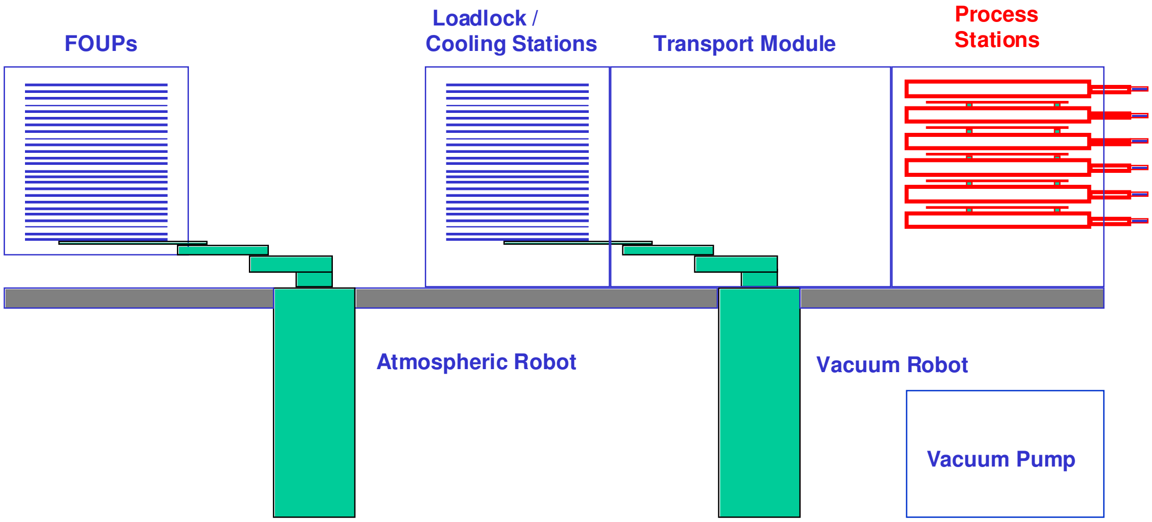


Fig. 4 Schematic diagrams of systems: (a) atmospheric system and (b) air tight system.

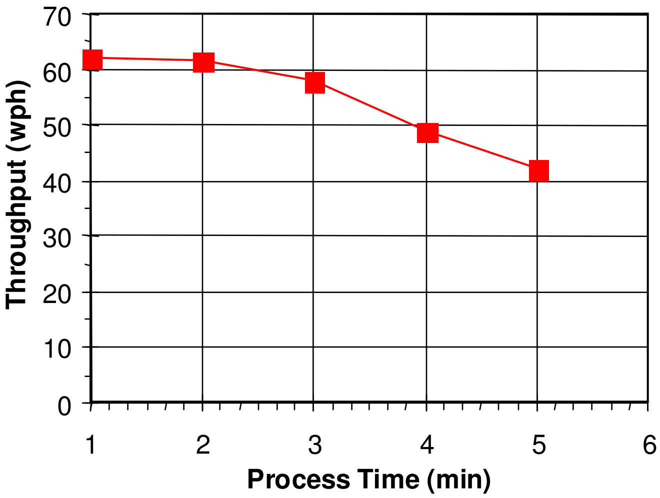
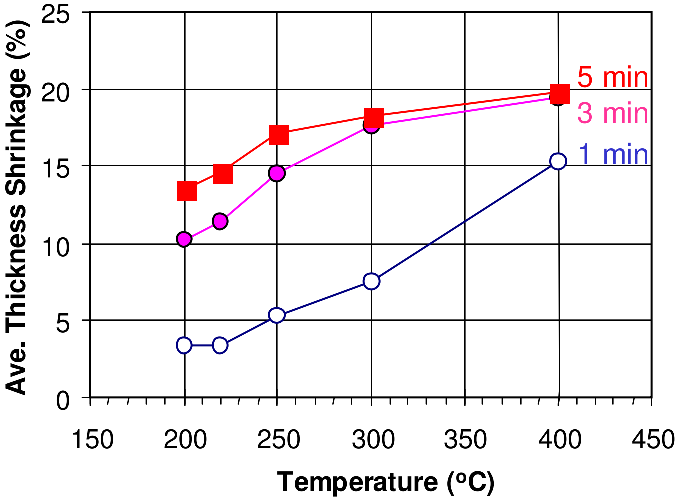


Fig. 5 Throughput of atmospheric system as a function of process time.


Ave. Thickness Shrinkage (%)
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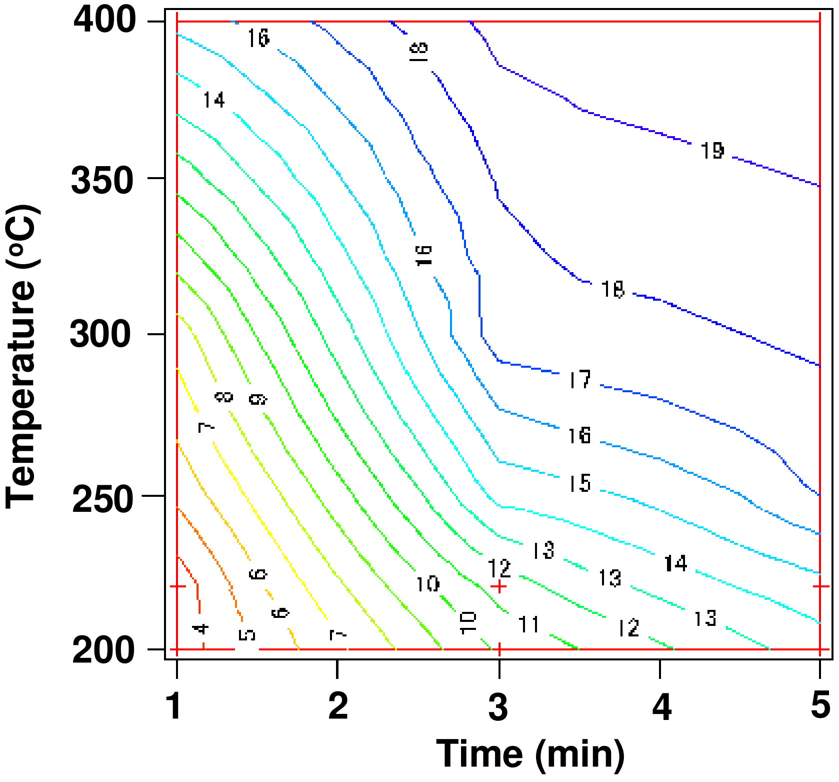
15
20
25
150
200
250
300
350
400
450
Temperature (°C)
5 min
3 min
1 min


Film Thickness Shrinkage (%)
Temperature (°C)
200
250
300
350
400
Time (min)
1
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6
6
7
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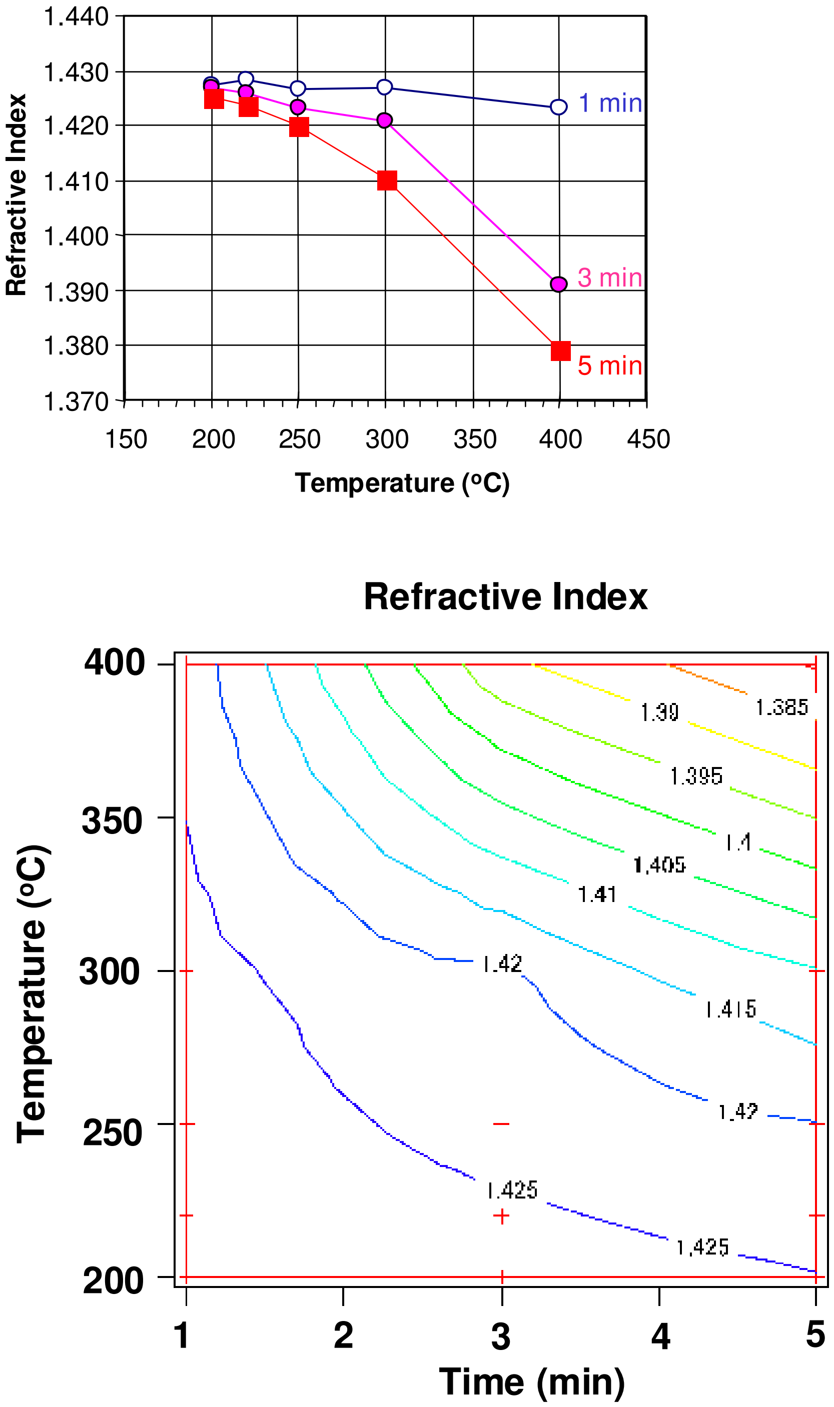

Fig. 6 Average thickness shrinkage (a and b) and refractive index (c and d) as a function of annealing temperature and time.

Biographies:

Woo Sik Yoo is chief technical officer and co-founder of WaferMasters, Inc. He has served as a research and process engineer at ATMI, Novellus Systems, and Lam Research, followed by positions as senior product technologist and product marketing manager at Mattson Technology. He has written more than 80 papers on RTP, dielectric PECVD, and wide band-gap compound semiconductors. He holds a BS degree in electronic engineering from Dongguk University in Korea, MS and PhD degrees in electrical engineering from Kyoto University, and an MBA degree from Western Connecticut State University. WaferMasters, Inc., 246 East Gish Road, San Jose, CA 95112; ph 408/451-0856, fax 408/451-9729, e-mail woosik.yoo@wafermasters.com

Taro Yamazaki is president and CEO of WaferMasters, Inc., and one of its co-founders. He has more than 20 years of international business experience in the semiconductor industry. He has served as director of market development for Mattson Technology and general manager of the export department for Marubeni International Electronics. He holds a BS degree in mechanical engineering from the Ashikaga Institute of Technology in Japan.

Toshiyuki Uchino is senior manager of Manufacturing Technology Department of Trecenti Technologies, Inc. He worked at Hitachi for 15 years as an equipment engineer of thermal process. He had contributed to development of vertical diffusion furnace. He holds a BS degree in mechanical engineering from the University of Tokyo and a MS degree in manufacturing systems engineering from the University of Wisconsin-Madison.