Low Temperature Batch Annealing Oven and Its SOG Annealing Application

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Biography:
Dr. Yoo is CTO of WaferMasters, Inc. and one of the co-founders. He has served as a Research and Process Engineer at ATMI, Novellus Systems and Lam Research, followed by positions as Senior Product Technologist and Product Marketing Manager at Mattson Technology. He has written more than 100 papers on RTP, dielectric PECVD and wide bandgap compound semiconductors. He holds a BS degree in Electronic Engineering from Dongguk University, Korea, MS and Ph.D degrees in Electrical Engineering from Kyoto University, Japan and an MBA degree from Western Connecticut State University .

Abstract:
A resistively heated batch annealing oven using stacked hot plates was proposed for low temperature (100~450°C) annealing applications. Thermal properties of the batch annealing oven using stacked hot plates were investigated. Wafer temperature profiles during low temperature annealing in stacked hot plates were characterized as a function of hot plate temperature, standoff height and process atmosphere. Spin-on-glass (SOG) films were annealed in the batch annealing oven. Changes in physical properties of SOG films before and after anneal was characterized as a function of temperature and time. Productivity and lot size flexibility of the batch annealing oven are compared with conventional hot plates and furnaces. The batch annealing oven which employs stacked hot plates is also very promising for low temperature annealing processes such as Cu anneal, Al anneal, low k dielectrics anneal, and photoresist baking applications.

Data:
- Introduction
Traditionally, low temperature annealing was done in batch furnaces. Typical batch size is ranging from 150 to 200 wafers. Due to the inflexibility in lot size and long cycle time, single wafer processing is preferred. For 300mm wafer processing applications, single wafer processing capability is essential from the viewpoints of cycle time reduction and risk management. In thermal processing applications above 600°C, lamp-heated single wafer RTP systems are frequently used. Accurate and reliable wafer temperature measurement/control below 600°C using optical pyrometry is difficult due to transparent optical property of Si in the IR region. In addition to the difficulty in wafer temperature measurement/control below 600°C using optical pyrometry, degradation of lamps and out gassing during annealing make process control even more difficult.

A good understanding of the thermal effect on wafers is essential to determine process parameters and design suitable processing equipment. Within-wafer and wafer-to-wafer temperature uniformity and repeatability are considered to be the most important process parameters to be monitored and controlled to assure process results. Since wafer warpage during temperature change can cause significant damage in device wafers, thermally induced stress has to be reduced as much as possible. A new concept annealing systems needed to be developed for low temperature annealing applications.

In this paper, a resistively heated hot plate system was proposed for low temperature (100~450^{o}C) annealing applications such as SOG anneal, Cu anneal, Al anneal, low k dielectrics anneal, and photoresist bake.

- *Heat transfer mechanism (< 600^{o}C)*

There are three heat transfer mechanisms. They are conduction, convection and radiation. The conduction heat transfer takes place at any temperature as long as the heat conduction media exist. The convection heat transfer occurs in liquid and gas media due to the temperature dependence of density of media. The radiation heat transfer does not require media and is determined by optical interaction between objects. Due to the bandgap energy of Si (1.1eV), Si only absorbs photons with energy higher than the bandgap energy. The absorption edge of Si is located around 0.96μm in wavelength. Consequently, Si is optically transparent in the IR region. As Si temperature increases, concentration of thermally generated electron-hole pairs increases exponentially. Si becomes optically opaque in the IR region around 600^{o}C. The radiation heat transfer is negligible when Si temperature is far below 600^{o}C and wavelength from heat source is longer than 0.96μm. The wavelength of visible light is between 0.4 ~0.7μm. For low temperature annealing applications below 600^{o}C, the conduction and convection heat transfer have to be considered in heat source design.

- *Batch annealing oven*

Resistively heated hot plates were used to heat 200mm and 300mm Si wafers in this study. Figure 1 shows a side view and top view of stacked hot plates with five Si wafers. The system is designed to process five wafers simultaneously. This feature allows gradual heating of wafers required for low temperature annealing/baking applications without deteriorating productivity. The individual hot plate is made of aluminum and has an embedded heater. The aluminum was chosen as the hot plate material because of its thermal stability in the temperature range up to 450^{o}C, high thermal conductivity and ease of machining. The hot plate is slightly larger than the Si wafer in diameter and significantly thicker (30mm) than the Si wafer. A thermocouple is embedded in the hot plate to measure and control the hot plate temperature during annealing. Each individual hot plate has three standoffs to keep the distance between a wafer and the hot plate. The standoffs are equally spaced on the perimeter of approximately 70% of wafer diameter. The gap between the hot plates is 20mm.

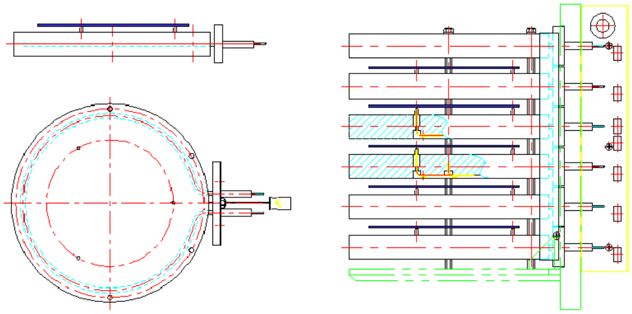

Fig. 1 Top and side view of stacked hot plates with five wafers.

The temperature uniformity of the hot plates was found to be very uniform. High thermal conductivity of aluminum prevents temperature gradient across the hot plates. The thermal conductivity of gases is 3 to 4 orders of magnitude lower than that of aluminum. [1] The poor thermal conductivity of gases makes heat dissipation through the gas phase conduction smaller. The stacked hot plate configuration makes convection between hot plates negligible and provides nearly isothermal environment for the wafer.

Wafer temperature profiles on hot plates were investigated as a function of hot plate configuration, standoff height, hot plate temperature and process atmosphere. [2] 300mm bare Si wafers with instrumentation thermocouples were annealed in the stacked hot plates at different temperatures under 1 atm air and He. The temperature of the six hot plates was controlled individually, but the temperature set points were kept the same. The wafer was placed on 8mm tall standoffs of the bottom hot plate. Temperature profiles of a wafer in stacked hot plates were measured at hot plate temperature set points of 100, 200, 300 and 400°C. Figure 2 shows the wafer temperature ramp up profiles in the stacked hot plates.

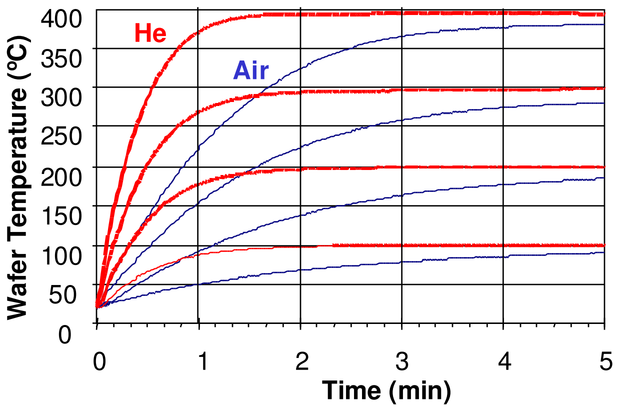

Fig. 2 Wafer temperature profiles under different process gas environment.

As soon as the wafer is inserted in the stacked hot plates, the wafer temperature initially increases almost linearly and then it saturates at little below the hot plate temperatures. Since the conduction heat transfer is one of the major heat transfer mechanisms at 1 atm air, the wafer temperature ramp up/down profile depends on ambient gas. When a high thermal conductivity gas such as H_2 and He is used, the wafer temperature ramp rate and the saturated wafer temperature are higher than air, N_2, O_2 and Ar. The heat transfer between the hot plates and the wafer is predominated by thermal conduction through the gas. The thermal conductivity of air and He gas at 300K under 760Torr are 26.2×10^{-5} and 156.7×10^{-5} W/cmK, respectively. [1] The thermal conductivity of gases increases with temperature. The thermal conductivity of air and He gas become 45.7×10^{-5} and 252.4×10^{-5} W/cmK at 600K under 760Torr. [1] Wafer temperature ramp rate varies with the hot plate temperature, standoff height, process pressure and process atmosphere.

The direct contact between a wafer and a hot plate provides fast wafer temperature ramp up, but it makes uniform wafer heating during temperature ramp up difficult. Wafers directly on a hot plate tend to slide during annealing when they out gas. By keeping an intentional gap between the hot plates and the wafer, good within wafer temperature uniformity can be obtained throughout the process. Wafer sliding can also be prevented. The wafer temperature profiles suggest that non-contact thermal annealing is gentle and provides repeatable process results. A nearly warpage free thermal annealing is achieved by placing a wafer on standoffs in stacked hot plates. [2] A stacked hot plate system is very promising for wafer warpage sensitive and out gassing low temperature annealing processes such as Cu anneal, Al anneal, SOG anneal, and photoresist baking applications. [3]

- SOG process results

SOG annealing was done using the batch annealing oven. Changes in physical properties of SOG films before and after anneal was characterized as a function of temperature and time. Organic SOG films on 200mm Si wafers with as spun thickness of 360nm were baked in the 5 wafer batch annealing oven under 1 atm air. The annealing temperature was varied from 200°C to 400°C. The annealing time was also varied between 1 and 5 min. The film thickness shrinkage and refractive index change after annealing under different conditions were measured (Fig. 3). As annealing temperature and time increase, thickness shrinks more and refractive index decreases due to the film densification. Thickness shrinkage up to 20% was obtained. Average thickness uniformity of SOG films after annealing ranges from 0.5 to 1.5% in 1σ.

Refractive index and SOG thickness uniformity after anneal are plotted in Fig. 4 as a function of average thickness shrinkage. Data points were collected in a wide range of annealing conditions (200°C~400°C, 1~5 min). The refractive index and uniformity of shrinkage show very strong correlation with the average thickness shrinkage of SOG films regardless of annealing temperature and time. Complete out gassing without generating cracks in SOG films is desirable. To achieve this process goals, uniform and gradual heating of Si wafer for relatively long time (4~5min) is desirable. Incomplete baking or nonuniform baking result in poor uniformity in selectivity of etch rate in the following etch back process step. We were able to control SOG film properties using the batch annealing oven in the wide range of process conditions.

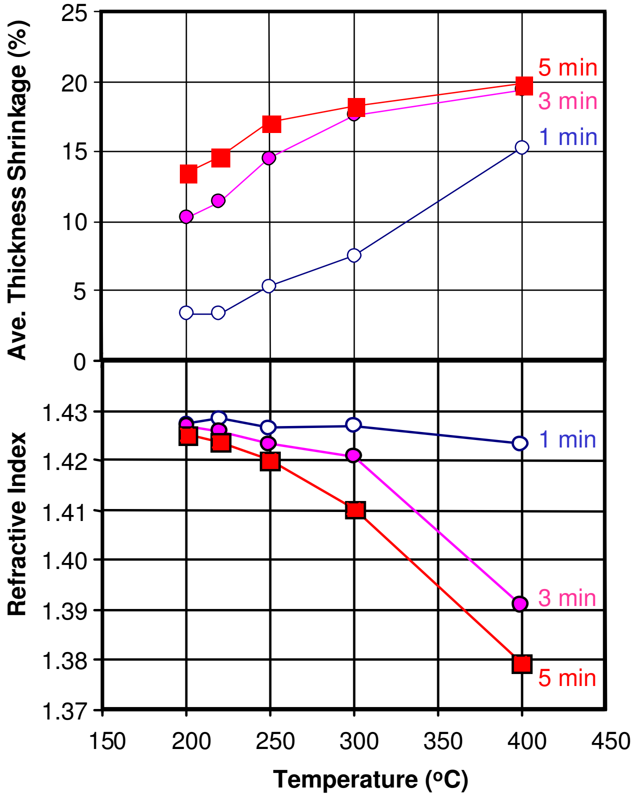

Fig. 3 SOG thickness shrinkage and refractive index under various annealing conditions.

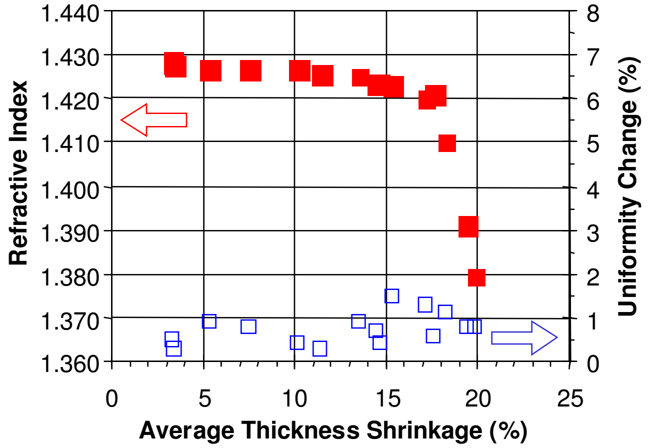

Fig. 4 Correlation among thickness shrinkage, refractive index and thickness uniformity change after annealing.

Due to the 5 wafer simultaneous processing capability and gentle wafer temperature ramp up characteristics of the system, we are able to achieve very repeatable process results at higher productivity compared to conventional single hot plates and batch furnaces. Lot size flexibility is also improved compared to the batch furnaces without deteriorating productivity. Typical throughput for 3~5min process is 60~40wph. While throughput is maintained to a comparable level to conventional large batch furnaces, we were able to reduce wafer cycle time significantly and improved the lot size flexibility. The throughput and process results (i.e. uniformity and repeatability) are improved significantly compared to conventional single hot plates. Figure 5 shows a schematic diagram of 300mm 5 wafer batch annealing oven with two FOUP opener. The system dimension is 1050mm (W) x 1600mm (D) x 2000mm (H) including two FOUP openers. The system used in this study does not require any process gas, compressed air or cooling water.

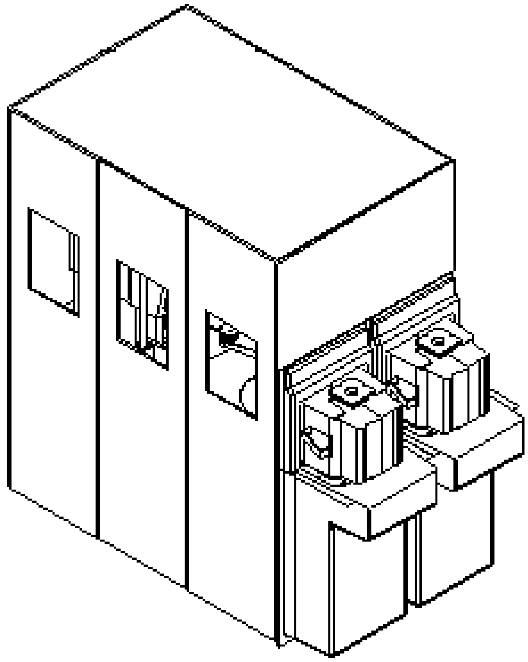

Fig. 5 Schematic diagram of 300mm batch annealing oven with two FOUP opener.

- Other process applications

The batch annealing oven which employs stacked hot plates is also very promising for low temperature annealing processes such as Cu anneal, Al anneal, low k dielectrics anneal, and photoresist baking applications. Chamber enclosure, process gases, vacuum pump and pressure control function can be added for processes which require precise process environment control.

Conclusion:

A resistively heated 5 wafer batch annealing oven using six stacked hot plates was proposed for low temperature (100~450°C) annealing applications. Thermal properties of the batch annealing oven using stacked hot plates were investigated. Wafer temperature profiles during low temperature annealing in stacked hot plates were characterized as a function of hot plate temperature and process atmosphere. SOG films were annealed in the batch annealing oven. Changes in physical properties of SOG films before and after anneal was characterized as a function of temperature and time. Productivity and lot size flexibility of batch annealing oven are compared with conventional hot plates and furnaces. The batch annealing oven which employs stacked hot plates is found out to be very promising for low temperature annealing processes such as Cu anneal, Al anneal, low k dielectrics anneal, and photoresist baking applications.

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