Design of a Hot Wall-Based Low Temperature Annealing System and Its Process Applications

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A hot wall-based low temperature annealing system using resistively heated, stacked hot plates was designed and tested for low temperature (100~500°C) annealing applications for 200mm and 300mm wafers. The system is designed to process five wafers simultaneously for productivity enhancement purposes. Thermal properties of the system and wafer temperature profiles during low temperature annealing in stacked hot plates were characterized as a function of hot plate temperature. The stacked hot plate configuration with proper gap between wafer and surrounding hot plates makes convection heat transfer predominant and provides uniform and repeatable process results in the low temperature region. Process uniformity and repeatability of NiSi formation, Cu annealing, Al sintering, spin-on-dielectrics (SOD) anneal were confirmed in the temperature range of 100~500°C.

INTRODUCTION

Silicon wafers are exposed to various thermal environments during the device fabrication process. As the device size shrinks and the device fabrication process becomes more complex, the number of low temperature annealing steps increases. The low temperature annealing steps for nickel silicide (NiSi) formation, copper (Cu) annealing and low κ dielectrics annealing in the temperature range of 100°C~500°C are some of the most critical steps for the technology nodes of 90nm and below. [1-9] Precise temperature and process ambient control are required. Both lamp-based RTA systems and large batch furnaces have difficulty in meeting the temperature uniformity and process environment requirements without significant hardware and control algorithm modifications.

A good understanding of the heat transfer mechanism and thermal effect on wafers in the temperature range of 100°C~500°C is essential to determine process parameters and design suitable processing equipment for low temperature annealing applications. Potential problems associated with the lamp-based RTA system or large batch furnaces in low temperature annealing applications under process ambient control are reviewed. To overcome and avoid these problems, we have designed a hot wall-based low temperature annealing system for 200mm and 300mm wafer annealing to address applications below 500°C under a controlled process ambient.

In this paper, heat transfer mechanisms are described for the temperature range of 100~500°C, system design considerations and wafer temperature profiles. The process performance of the system is demonstrated by analyzing the within wafer and wafer to wafer uniformity and repeatability data with correlation to NiSi formation, Cu annealing and spin-on-dielectrics (SOD) densification process results.

ANNEALING SYSTEM

Design of Annealing System

A resistively heated, stacked hot plate system was designed and tested for low temperature annealing applications in the temperature range of 100~500°C. [1, 4] The stacked hot plate system was designed to provide single wafer signature, lot size flexibility and reasonable productivity at minimum facility requirement. Resistively heated hot plates were used to heat 200mm and 300mm Si wafers in this study. The system is designed to process five wafers simultaneously. Figure 1 shows a side view of stacked hot plates with five Si wafers. This feature allows gradual heating of wafers required for low temperature annealing and baking applications without reducing productivity. The individual hot plate is made of aluminum and has an embedded heater for temperature control.

Aluminum was chosen as the hot plate material because of its thermal stability in the temperature range up to 500°C, high thermal conductivity and ease of machining. The hot plate is slightly larger than the Si wafer in diameter and significantly thicker than the Si wafer. Individual hot plates have three standoffs to maintain the spacing between wafer and the hot plate. The standoffs are equally spaced on the perimeter of approximately 70% of wafer diameter. During process, wafers are placed on the standoffs on the bottom of each hot plate. Thus, wafers are located precisely halfway between the top and bottom hot plates.

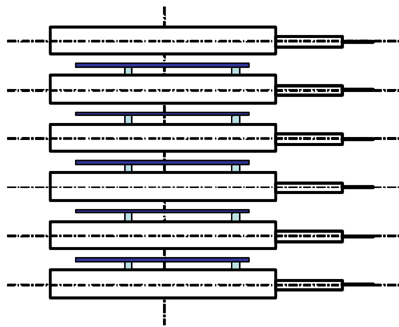

Fig. 1 Schematic diagram of stacked hot plates.

Characterization of Annealing System

The temperature uniformity across the hot plates is very uniform because of the high thermal conductivity of aluminum. The stacked hot plate configuration makes convection between hot plates negligible and provides a nearly isothermal environment for the wafer. As the thermal conductivity of gases is 3 to 4 orders of magnitude lower than that of aluminum. [10] The poor thermal conductivity of the ambient gas makes heat loss from the hot plates to environment quite small.

Temperature ramp up profiles of 200mm Si wafers in the stacked hot plates were measured as a function of hot plate temperature and process atmosphere. [1, 5] Bare Si wafers with instrumentation thermocouples were inserted between the stacked hot plates at different temperatures under 1 atm in an air and He mixture. The temperature set point of the six hot plates was kept the same and the hot plate temperature was controlled individually. Temperature profiles of a wafer between stacked hot plates were measured at hot plate temperature set points of 100, 200, 300 and 400°C. Figure 2 shows the wafer temperature ramp up profiles between the stacked hot plates. Temperature uniformity within wafer and slot-to-slot across the 5 wafer load was within +/- 1°C.

As the wafer is inserted in the stacked hot plates, the wafer temperature increases gradually and saturates at slightly below the hot plate temperature. The predominant heat transfer mechanisms between the hot plates and the wafer are thermal convection and conduction through the gas. The wafer temperature ramp up profile depends on ambient gas specifics. When a high thermal conductivity gas such as H_2 and He is used as an ambient gas, the wafer temperature ramp rate and the saturated wafer temperature are higher than for air, N_2, O_2 and Ar. [10]

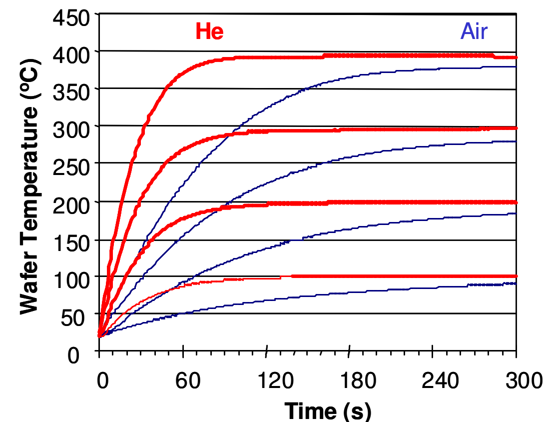

Fig. 2 Temperature ramp up profiles of a 200mm Si wafer during annealing process under a 1 atm air and He mixture.

The direct contact between a wafer and a hot plate provides fast wafer temperature ramp up, but also results in thermal shock and uneven wafer heating during temperature ramp up. When wafers with films deposited or coated at low temperatures are directly placed on a hot plate, they tend to slide during annealing due to the air bearing effect of out gassed species. By keeping an intentional gap between the hot plates and the wafer, good within wafer temperature uniformity can be obtained throughout the process. Wafer sliding can also be prevented. The wafer temperature profiles suggest that non-contact thermal annealing is gentle and provides repeatable process results. Thus, nearly warpage-

free thermal annealing is achieved by placing a wafer on standoffs between stacked hot plates.

PROCESS RESULTS

Cu Annealing (100°C~450°C)

The sheet resistance of Cu films on blanket wafers was measured before and after annealing in a forming gas atmosphere. Figure 3 shows sheet resistance reduction in 3.0 µm thick Cu films on blanket wafers as a function of annealing temperature and time. As annealing temperature and time increase, the sheet resistance was reduced drastically regardless of Cu film thickness. When the annealing temperature exceeded 200°C or the annealing time exceeded 5 min, the sheet resistance was reduced by 21~23% from the original sheet resistance. Uniformity change before or after annealing was below 1 % in 1σ. [6, 7]

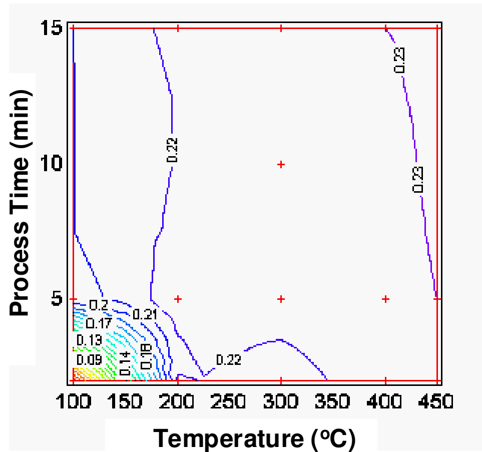

Fig. 3. Surface response of the sheet resistance reduction ratio of Cu films (3.0µm thick) as a function of annealing temperature and time.

NiSi Annealing (250°C~500°C)

Sputtered Ni films (9 nm thick) on Si wafers were annealed in the temperature range of 200~500°C to form nickel silicide. The sheet resistance of nickel silicide was measured before and after annealing (Fig. 4). Ni_2Si formation was observed as low as 200°C. The sheet resistance was increased from 25.8 ohm/sq. to 36.0 ohm/sq. after annealing at 200°C for 5 minutes due to Ni_2Si formation. As the annealing temperature increased, the sheet resistance sharply decreased to ~10 ohm/sq. above 300°C by forming a lower resistivity NiSi phase. The uniformity change before and after annealing was also below 1 % in 1σ. [8, 9]

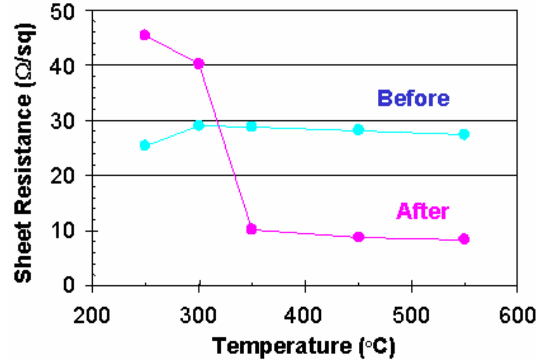

Fig. 4. Sheet resistance change of Ni films (9.0nm thick) before and after annealing at different annealing temperatures.

Spin on Dielectrics Annealing (200°C~400°C)

Complete out gassing without generating cracks or blisters in films is desirable for baking and curing of SOD materials. To achieve this process goal, uniform and gradual heating of Si wafer for a relatively long time (4~5min) is desirable. Incomplete or nonuniform baking results in poor uniformity in selectivity of etch rate in the subsequent etch back process step.

We were able to achieve the desired siloxane-based SOD film properties after annealing using the low temperature annealing system under a wide range of process conditions. Surface responses, plot of film shrinkage and refractive index after annealing under various process temperatures and times, are shown in Fig. 5. As annealing temperature and time increase, thickness shrinks and refractive index decreases due to film densification. Thickness shrinkage up to 19% was obtained. Average thickness uniformity of SOG films after annealing ranges from 0.5 to 1.5% in 1σ. Surface response patterns of film shrinkage and refractive index look quite similar. This suggests a strong correlation between film shrinkage and refractive index. Typical refractive index of as spun SOD films range from 1.426 to 1.428. As annealing temperature and time increases, the film shrinks and the refractive index decreases. The refractive index of completely densified SOD films at

400°C for 5 min is around 1.390. Typical refractive index for thermally grown oxide is 1.460. [2 - 4]

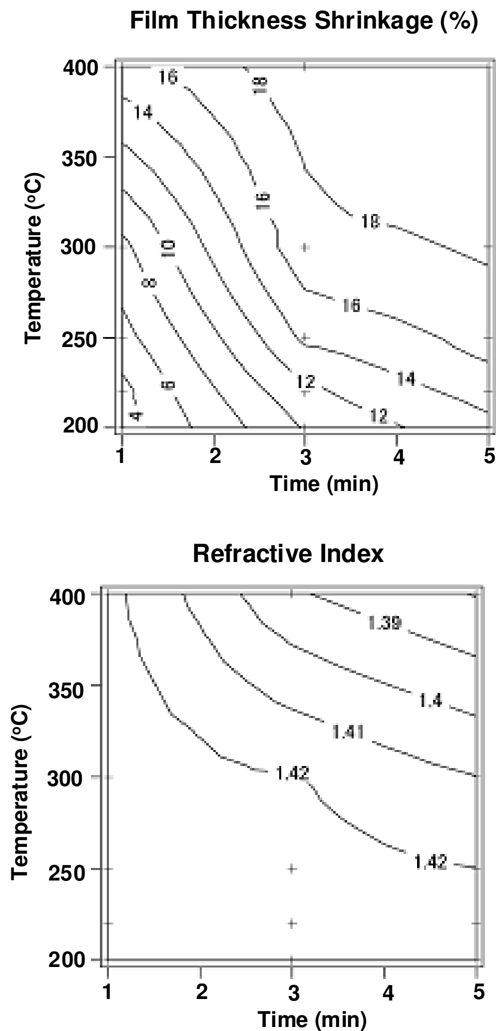

Fig. 5. Surface response plots of film shrinkage and refractive index of SOD films after annealing under various process temperature and time.

DISCUSSION

As device design rules continue to shrink, precise control of process parameters such as annealing temperature, annealing time and process ambient is required. To make thermal processing as robust as possible, potential temperature error and overshoot have to be reduced. Low temperature thermal processing has been one of the challenging areas for the future device technology nodes (90 nm and beyond) due to the introduction of new materials and their limitation of maximum processing temperature. Ideal temperature measurement and control strategy is discussed below.

Optical pyrometry is frequently used for measuring Si wafer temperature in lamp-based RTP systems as a non-contact temperature measurement technique. It has significant drawbacks in measurement range and accuracy. The optical properties of Si as well as film stacks must be considered when measuring or heating Si wafers by optical means.

Wafer temperature measurement below 600°C is not reliable using optical pyrometers because the optical properties of Si in the infrared region drastically change in the temperature ranges between room temperature and 600°C. In addition, the light output from Si is very weak. As a result, the signal-to-noise (S/N) ratio is very small (i.e. temperature measurement error is significant below 600°C). Difficulty with temperature measurement and overshooting make this method less suitable for a mass production environment from the process quality control point of view.

Even above 600°C, the measurement is strongly influenced by the local and global optical property variations within wafer and wafer-to-wafer due to inconsistencies in dopant concentration, device patterns, backside films etc. The emissivity of Si is a function of temperature. Without knowing the local and global emissivity distribution of a wafer, it is very difficult to measure and control wafer temperature accurately. The measured temperature value can differ from the true value when line-of-sight measurement is blocked or the optical property of the media, such as the window, is affected (often caused by condensation or coating of materials on the window). This can cause process shifts without any warning.

There are two types of wafer temperature control methods. The first one is dynamic wafer temperature control using in-situ wafer temperature measurement values. Typical lamp based-RTP systems employ this technique. The second one is an environment temperature control method. Instead of controlling the wafer temperature directly, the temperature of the

process chamber, the wafer's environment, is controlled. The wafer temperature naturally approaches the process environment temperature without overshoot. This method is less sensitive to the optical properties of a Si wafer with film stacks. This method provides very repeatable process results compared to those using the direct wafer temperature control method. Typical furnaces fall into this category. They can also be classified as a cold wall system or hot wall system.

For low temperature processing applications, heat source temperature measurement using a thermocouple is suitable because (1) the intensity of the thermocouple output signal is proportional to the temperature difference between the heat source and reference, (2) the variation of optical properties of wafers does not induce temperature measurement errors and (3) wafer temperature overshoot is not possible.

SUMMARY

For low temperature (100~500°C) annealing applications for 200mm and 300mm wafers, a hot wall-based low temperature annealing system using resistively heated, stacked hot plates was designed and tested for NiSi formation, Cu annealing and SOD annealing applications. The system is designed to process five wafers simultaneously for productivity enhancement without rushing process steps for productivity increase at a cost of process quality. Thermal properties of the system and wafer temperature profiles during annealing in stacked hot plates were characterized as a function of hot plate temperature and annealing time. The stacked hot plate configuration with proper gap between wafer and surrounding hot plates makes convection heat transfer predominant and provides uniform and repeatable process results in the low temperature region. Process uniformity and repeatability of NiSi formation, Cu annealing, SOD anneal were confirmed in the temperature range of 100~500°C.

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