Comparative Study on Implant Anneal using Single Wafer Furnace and Lamp-based Rapid Thermal Processor

Woo Sik Yoo[1], Takashi Fukada[1], Tsuyoshi Setokubo[2], Kazuo Aizawa[2],
Toshinori Ohsawa[3], Nobuaki Takahashi[4] and Ryuichi Komatubara[4]

[1] WaferMasters, Inc., 246 East Gish Road, San Jose, CA 95112 U.S.A.
[2] NEC Hiroshima Limited
5690 Yoshikawa, Happonmatsu, Higashi Hiroshima, Hiroshima, 739-0198 Japan
[3]Tokyo Electron FE Ltd, 30-7 Sumiyoshi-cho 2-chome, Fuchu, Tokyo 183-8705 Japan
[4]Tokyo Electron Ltd, 3-6 Akasaka 5-chome, Minato-ku, Tokyo, 107-8481, Japan

Comparative study on rapid thermal annealing (RTA) of various implant species ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$) in 200mm diameter Si wafers was done using a single wafer furnace (SWF) system and a lamp-based RTP system under 1 atm N_2 atmosphere. Average sheet resistance and its uniformity were measured after annealing under various conditions. Production worthy process windows for SWF and lamp-based conventional RTA systems are also compared. Lower average sheet resistance and superior sheet resistance uniformity were achieved in wide process conditions using SWF system. Effect of annealing on dopant redistribution was investigated using secondary ion mass spectroscopy (SIMS). The validity of "spike anneal" was discussed based on electrical activation and dopant diffusion mechanisms in implanted Si wafers.

INTRODUCTION

As device dimensions and junction depth decrease, rapid thermal processing (RTP) is believed to be the only solution for implant anneal. Racing for higher wafer temperature ramp rate and shorter process time between RTP system manufacturers had begun a few years ago. For RTP of a 200 mm diameter wafer, numerous tungsten halogen lamps are used. Wafer temperature ramp up rate of ~250°C/s and process time as short as 0s (named as "spike anneal") are applied in annealing of implanted wafers. [1-2] Implanted wafers are often annealed above 1000°C for 0~60s in RTP systems while they are annealed between 800°C and 950°C for 10~30min in conventional batch furnaces. [3]

The authors had fundamental question regarding the effect of annealing temperature and annealing time on implant activation efficiency. Recently, a new RTP approach using single wafer type furnace has been proposed and its thermal characteristics and preliminary process results haven been reported. [3-6] The single wafer furnace (SWF) allows short time annealing in nearly isothermal furnace environment. In this paper, the authors carried out comparative study on the effect of annealing temperature and annealing time on implant activation efficiency using the SWF system and conventional lamp-based RTP system.

In this paper, rapid thermal annealing (RTA) of various implant species ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$) in 200mm diameter Si wafers was done using the SWF system and a lamp-based RTP system under 1 atm N_2 atmosphere to compare resulting sheet resistance and its uniformity after annealing. Production worthy process windows for SWF and lamp-based conventional RTA systems are also compared. Dopant depth profiles were investigated using secondary ion mass spectroscopy (SIMS).

EXPERIMENTAL

Single Wafer Furnace (SWF)

A dual chamber, SWF system with a vacuum loadlock is used in this study. Two vertically stacked process chambers (furnace), a vacuum loadlock and two cooling stations are attached to the wafer transport module. By stacking two furnaces, the footprint of the system is greatly reduced. The process tube has three standoffs made of quartz. The process tube uses no moving parts for simplicity and system reliability. The wafer is placed on the quartz standoffs (8~9mm tall) in the middle of quartz process tube. The distance between the wafer and the quartz walls is kept at ~10mm for both upward and downward directions. The quartz process tube is located in a SiC cavity which acts as heat distributor to create isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly. The temperature of the SiC cavity is monitored and controlled at a predetermined process temperature by three embedded R-type thermocouples and the three zone heater assembly to provide identical and nearly isothermal environment to wafers regardless of wafer types and conditions. Detailed configuration, thermal characteristics and process performance of the system has been reported elsewhere. [4-7]

Lamp-based RTA System

The lamp-based RTA system employs banks of linear tungsten halogen lamp array and illuminate a Si wafer through the quartz process tube from top and bottom sides. Wafer temperatures are measured using a pyrometer through the quartz tube. Multiple zone power control method is used to adjust temperature uniformity on a Si wafer. Wafer temperature ramp up rate, soak time and ramp down rate are programmable.

Implant Anneal

Paired experiments have been carried out using the SWF and lamp-based RTA systems in mass production environment after characterizing thermal characteristics of both systems. In this study, process time for the SWF system was determined by simply adding 30s to the "soak time" in lamp-based RTP system because it is equivalent to "ramp up time" plus "soak time" in the lamp-based RTP system (Fig.1).

200mm diameter Si wafers implanted with various species were annealed using the SWF system and lamp-based RTP system under 1 atm N_2 atmosphere to compare resulting sheet resistance and its uniformity after annealing. The annealing temperature was varied between 900°C and 1100°C. The annealing time for SWF system was varied between 40s and 180s. Accordingly, the annealing time for the lamp-based RTP system was varied between 10s and 150s. The sheet resistance of annealed wafers were measured at 49 points using a four-point probe. 5mm edge exclusion was used during the sheet resistance measurement. Surface response of sheet resistance and its uniformity were used for process window determination. Dopant depth profiles were also measured before and after annealing using SIMS for comparison.

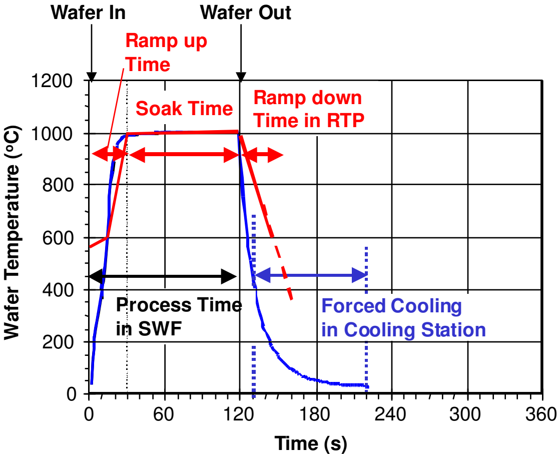

Fig. 1. Schematic illustration of wafer temperature profiles during 120s process in SWF system and 90s process in RTP system.

RESULTS AND DISCUSSIONS

Average sheet resistance and sheet resistance uniformity plots of four different types of implanted wafers ($^{11}B^+$ 50keV 1x10^{15} cm^{-2}, $^{49}BF_2^+$ 70keV 1x10^{15} cm^{-2}, $^{31}P^+$ 70keV 1x10^{15} cm^{-2} and $^{75}As^+$ 70keV 1x10^{15} cm^{-2}) were plotted in Figs. 2 and 3 as a function of process (annealing) temperature. Process results from the SWF and lamp-based RTP systems are shown in Fig. 2 and Fig. 3, respectively. Process (annealing) time was fixed at 70s (from wafer-in to wafer-out) for the SWF system and 30s (soak time at process temperature) for the lamp-based RTP system. All four kind of implanted wafers were electrically well activated above 1000°C regardless of wafer heating method (annealing system). Equivalent average sheet resistance values were achieved in wafers annealed using both systems. A higher temperature sensitivity of sheet resistance was observed in $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers compared to those in $^{31}P^+$ and $^{75}As^+$ implanted wafers.

The sheet resistance uniformity in all four different types of implanted wafers ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$) annealed at 900°C and 1000°C using the SWF system was below 1.0% (1σ). $^{49}BF_2^+$ and $^{75}As^+$ implanted wafers showed slight increase of sheet resistance uniformity values after annealing at 1100°C while the average sheet resistance value remain constant.

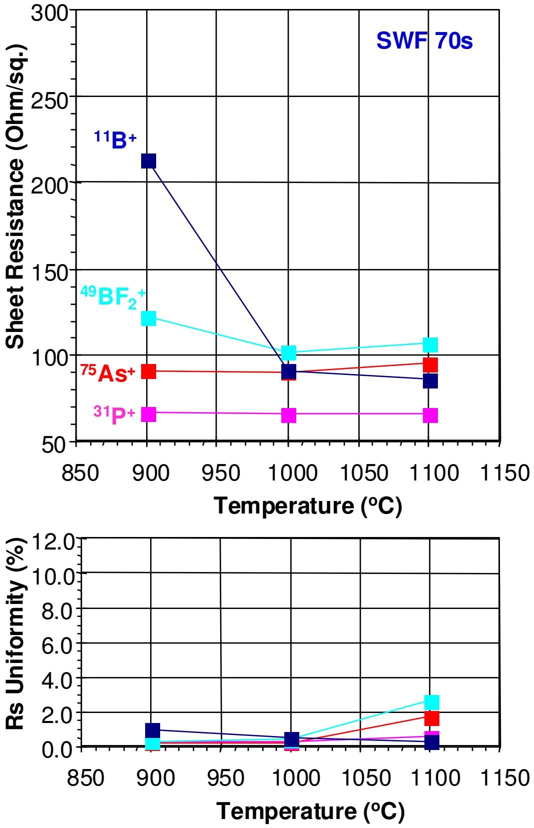

Fig. 2. Average sheet resistance and its uniformity of implanted wafers after annealing in SWF system.

In case of the lamp-based RTP system, all four different types of implanted wafers ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$) annealed at 1000°C showed the sheet resistance uniformity below 1.0% (1σ). At annealing temperatures of 900°C and 1100°C, sheet resistance uniformity values of most implanted wafers exceeded 1.0% (1σ). In case of $^{49}BF_2^+$ implanted wafers, both average sheet resistance and its uniformity values significantly increased after annealing at 1100°C. The average sheet resistance value was increased from 102.6 ohm/sq. at 1000°C to 146.4 ohm/sq. at 1100°C. The sheet resistance uniformity value in 1σ was also significantly increased from 0.25% (at 1000°C) to 10.22% (at 1100°C) after annealing.

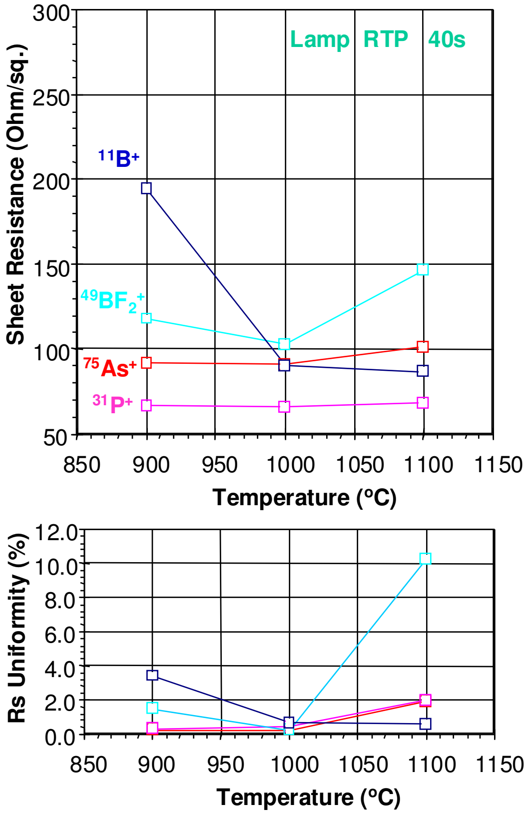

Fig. 3. Average sheet resistance and its uniformity of implanted wafers after annealing in lamp-based RTP system.

The average sheet resistance and sheet resistance uniformity of $^{11}B^+$ (50keV 1x10^{15} cm^{-2}) implanted wafers are shown in Fig. 4 and 5 as a function of annealing temperature and time. As seen in the figures, behavior of the average sheet resistance and sheet resistance uniformity in annealed wafers are very complex. In wafers annealed using the SWF system, sheet resistance decreases as annealing temperature and annealing time due to electrical activation of implanted species. As seen in the Figs. 2 and 3, the sheet resistance values are very sensitive to annealing temperature in the temperature range of 900°C and 1000°C regardless of annealing system. In terms of sheet resistance uniformity, the SWF system provides wide window for annealing conditions. Process windows for $^{11}B^+$

(50keV 1x10^{15} cm^{-2}) implanted wafers in the SWF system and lamp-based RTP system were determined by using the average sheet resistance value of <90ohm/sq. and the sheet resistance uniformity <0.5%(1σ) as criteria. The process windows in each systems are indicated in Fig. 4 and 5. The sheet resistance uniformity was the limiting factor for the process window in both SWF system and lamp-based RTP system. In general, longer annealing at lower temperatures gives lower average sheet resistance and better sheet resistance uniformity.

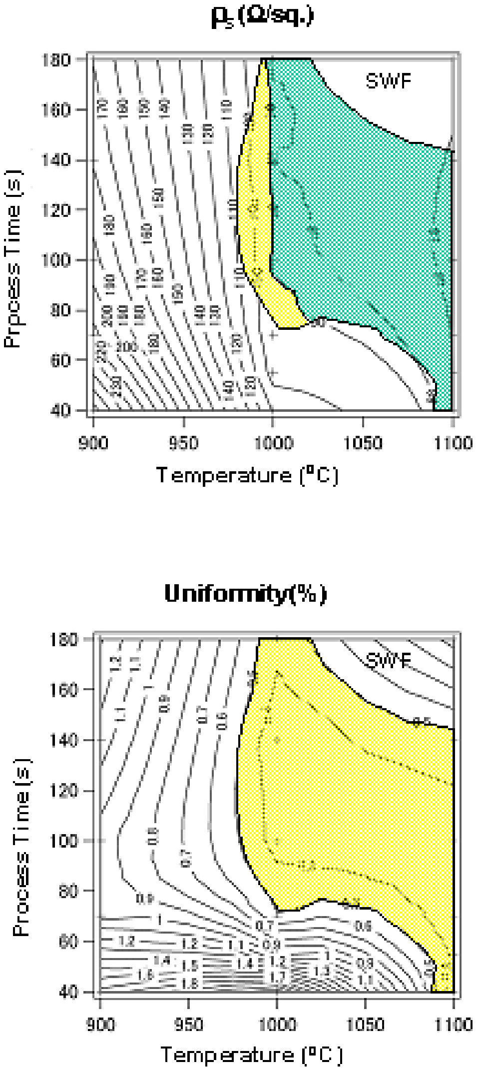

Fig. 4. Surface response maps and process window of average sheet resistance and its uniformity after annealing in SWF system.

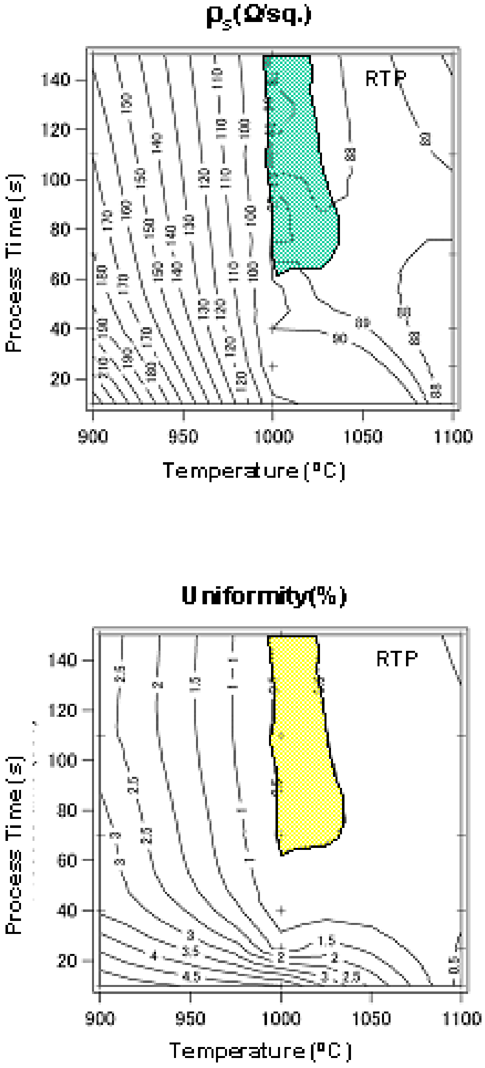

Fig. 5. Surface response maps and process window of average sheet resistance and its uniformity after annealing in lamp-based RTP system.

Figure 6 shows SIMS depth profiles of as implanted ($^{11}B^+$ 50keV, $1x10^{15}$ atoms/cm^2) wafer and wafers annealed at 1000°C in the SWF and lamp-based RTP systems. Annealing times for the SWF and lamp-based RTP systems were 100s (wafer-in to wafer-out) and 70s (soak time), respectively. Diffusion of boron atom toward the surface and depth direction was observed after annealing. Both average sheet resistance and SIMS depth profiles of wafers annealed using different types of annealing systems became very close to each other.

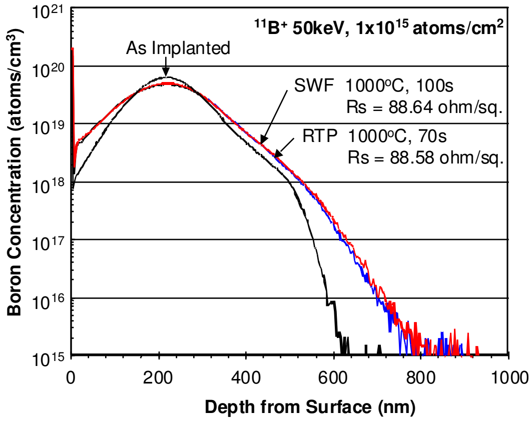

Fig. 6. SIMS depth profiles of as implanted wafer and wafers after annealing in SWF and lamp-based RTP systems.

$^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$ implanted wafers showed average sheet resistance increase with increase in annealing temperature (>1000°C) and time while $^{11}B^+$ implanted wafers showed decreases in average sheet resistance. The average sheet resistance increase with increase in annealing temperature and time can be explained by the thermal diffusion of implanted species in the wafer. As thermal diffusion progresses, the dopant concentration in the implanted region decreases and resulted in increase of the average sheet resistance.

To understand the physics behind the implant anneal, we need to review how the implant anneal is done in conventional batch furnaces. It takes place in temperature range of 800°C~950°C for 10~30min. Very consistent average sheet resistance and sheet resistance uniformity are achieved. However, the conventional batch furnace lacks lot size flexibility and requires longer cycle time.

Three main reactions take place in parallel during implant anneal. They are (1) recrystallization (solid phase regrowth) of damaged (amorphized) layer during implantation, (2) electrical activation of implant species and (3) thermal diffusion of implanted species. Full recrystallization of amorphized layer and full electrical activation of implant species without thermal diffusion would be ideal for implant anneal. It is well known that the solid-phase regrowth occurs temperature as low as 450°C. Solid-phase regrowth rates of (100) silicon at 600°C and 800°C are approximately 1nm/s and 500nm/s, respectively. [8] Electrical activation and dopant diffusion require higher thermal energy to take place. There are two well known facts: (1) diffusivity of atoms in Si increases exponentially as annealing temperature increases and (2) increase in diffusion length is propotional to square root of annealing time. [9]

To achieve maximum electrical activation with minimum dopant diffusion, implant annealing process must be optimized in terms of annealing temperature and annealing time. For the production-worthy repeatable process results on the average sheet resistance and sheet resistance uniformity, a reasonable amount of annealing time at an optimum temperature is desired rather than a "spike anneal" at maximum temperature.

We can conclude that the SWF system offers equivalent or better implant annealing process results and higher productivity compared to the lamp-based RTP system. The SWF system also offers single wafer signature, lot size flexibility and high energy efficiency. [4-7] Many RTP applications including implant anneal can be performed using the SWF system.

SUMMARY

Comparative RTA study of various implant species ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$) in 200mm diameter Si wafers was done using a resistively heated, SWF system and lamp-based conventional RTP system under 1 atm N_2 atmosphere. Average sheet resistance and sheet resistance uniformity were measured after annealing under various conditions. Production worthy process windows for SWF and lamp-based conventional RTP systems are also compared. Lower average sheet resistance and superior sheet resistance uniformity were achieved in wide process conditions using SWF system. Effect of annealing on dopant redistribution was investigated using SIMS. The validity of “spike anneal” was discussed based on electrical activation and dopant diffusion mechanisms in implanted Si wafers.

ACKNOWLEDGEMENTS

The authors would like to thank Mr. Y. Hiraga, Mr. K. Kang, Mr. S. Fujimoto and Mr. T. Yamazaki of WaferMasters, Inc. for useful discussions and encouragement throughout this work. The authors also would like to thank Mr. T. Shimotani, Mr. Y. Shirotani and Mr. J. Yamamoto of NEC Hiroshima Limited for the experimental arrangements.

REFERENCES

[1] D. Jennings, G. de Cock and M. A. Foad, Proc. 6th Int. Conf. on Advanced Thermal Processing of Semiconductors - RTP’98 (Kyoto, 1998) 187.

[2] A. J. Mayur, A. Jaggi and A. Jain, Proc. 8th Int. Conf. on Advanced Thermal Processing of Semiconductors- RTP 2000 (Gaithersburg, 2000) 196.

[3] S. Wolf and R.N. Tauber, *Silicon processing for the VLSI Era* Vol. 1 (Lattice Press, California 1986) Chap. 9.

[4] W.S. Yoo, T. Fukada, H. Kitayama, N. Takahashi, K. Enjoji and K. Sunohara: Jpn. J. Appl. Phys. Lett., **39** (2000), L493.

[5] W.S. Yoo, T. Fukada, H. Kuribayashi, H. Kitayama, N. Takahashi, K. Enjoji and K. Sunohara: Jpn. J. Appl. Phys. Lett., **39** (2000), L694.

[6] W.S. Yoo, T.Yamazaki and K. Enjoji, Solid State Technology, **43** No. 7 (2000) 223.

[7] W.S. Yoo, T, Fukada, H. Kuribayashi, H. Kitayama, N. Takahashi, K. Enjoji and K. Sunohara, Jpn. J. Appl. Phys. Vol. **39** (2000) 6143.

[8] V. E. Borisenko and P. J. Hesketh, *Rapid Thermal Processing of Semiconductors* (Plenum Press, New York and London, 1997) Chap. 2.

[9] W. R. Runyan and K.E. Bean, *Semiconductor Integrated Circuit Processing Technology* (Addison-Wesley Publishing Co., New York, 1990) Chap. 8.