Cobalt Silicide Formation Characteristics in a Single Wafer Rapid Thermal Furnace (SRTF) System

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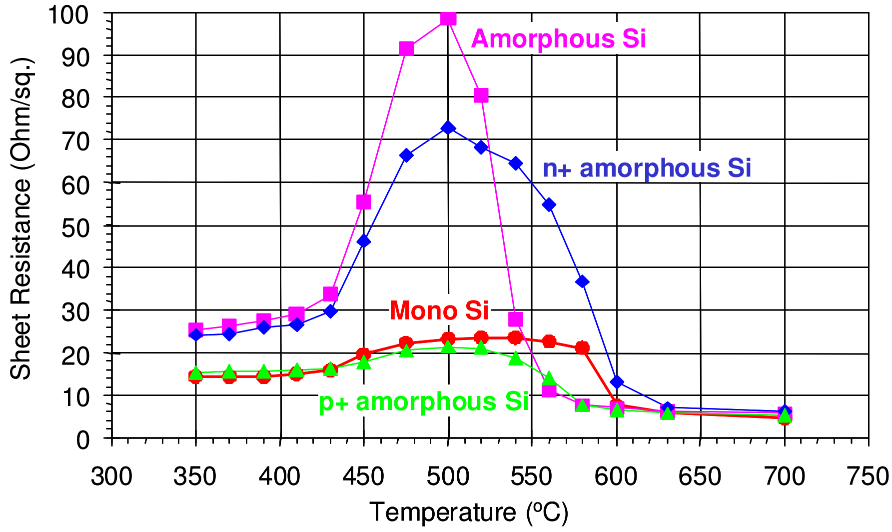
The formation of reliable and low resistance thin silicide contacts to Si is still a significant challenge for metal-oxide-semiconductor field effect transistors (MOSFETs) with small feature sizes (<110nm design rule). Compared to $TiSi_2$ contacts, $CoSi_2$ is particularly attractive to small scale device applications because of its ease of formation on narrow Si lines. Cobalt silicide is processed at lower temperatures (400~700°C). In this temperature regime, typical lamp heated RTP systems exhibit problems with temperature control, repeatability, and uniformity. The huge emissivity change observed in cobalt films during the thermal reaction process and local heating due to "pattern effect" make temperature control in lamp heated RTP systems very difficult. Alternative RTP techniques are being actively investigated to reduce the emissivity and pattern-related negative effect during silicide formation..

In this paper, very thin cobalt silicide formation and annealing were investigated using a rapid thermal furnace (SRTF) system. TiN (10nm thick) capped cobalt films (9nm thick) on four types of wafer surfaces (bare Si, amorphous Si and n^+ amorphous surface and p^+ amorphous surface) were investigated. Cobalt silicide process sensitivity was investigated in nitrogen ambient as a function of process temperature (350~700°C) and wafer surface. Process time (wafer residence time in a preheated nearly isothermal process chamber) was fixed at 90s for simplicity. The cobalt silicidation showed two characterization transitions, one at about 450°C and another at about 500~630°C representing two phase transitions during silicidation. The first transition temperature was at about 450°C regardless of wafer surface type. However, the second transition temperature was strongly influenced by the type of wafer surface. Figure 1 shows the sheet resistance and sheet resistance uniformity of TiN capped 9nm thick cobalt films. Except for the phase transition regions around 450°C and 500~630°C, the sheet resistance uniformity has improved after annealing.

Patterned wafers were processed for morphological and electrical characterization. Details of characterization will be presented at the conference.



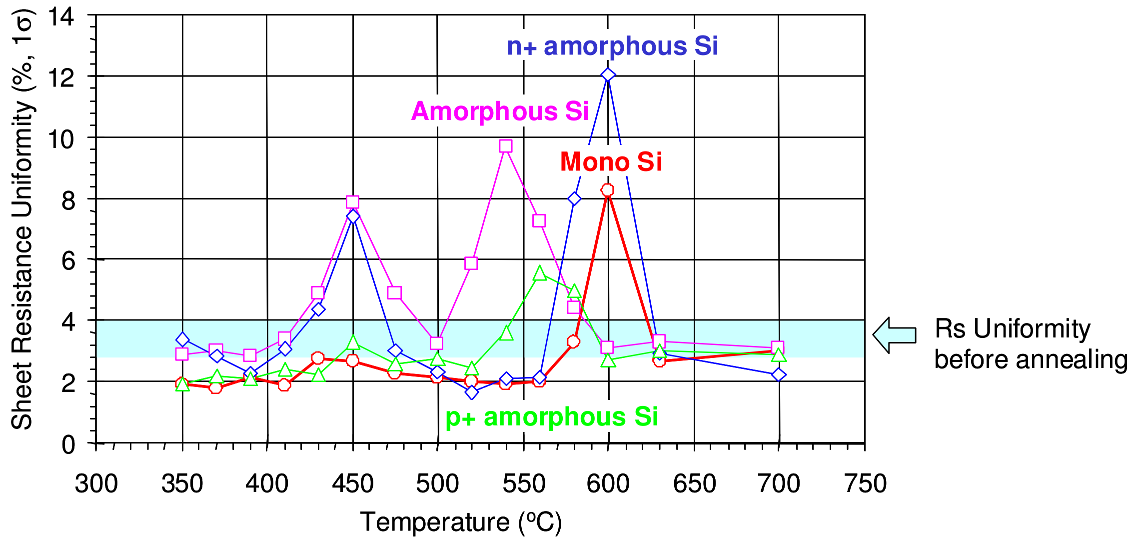


Fig. 1. Sheet resistance and sheet resistance uniformity of TiN capped 9nm thick cobalt films on various types of wafer surface.