

Optimizing the Formation of Nickel Silicide

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Abstract

A review of the formation processes for nickel silicide is given to assess the limitations of using the silicide for sub-65 nanometer technologies. Various aspects attributed to the NiSi formation process are described and addressed by using a two-step process sequence for annealing.

The focus of this study was to develop a process sequence with three principal steps to achieve low resistivity NiSi films utilizing a low temperature isothermal cavity based furnace. Process parameters for a low resistivity NiSi film were determined for a two-step annealing sequence to enhance device electrical characteristics. Through optimization of the initial anneal combined with a second higher temperature stabilization anneal, reduced defect levels are obtained resulting in reduced device leakage.

Introduction

Nickel silicide has taken on new importance for advanced technologies beyond the 65 nm technology node. Lower formation temperature and silicon consumption overcome the limitations of CoSi₂ and its scaling ability provides a platform for extending into the 30 nm technology range. For successful implementation, key material and formation limitations need to be characterized to minimize the effects on the devices' electrical characteristics. This paper reviews several aspects of NiSi films and their

formation processes to minimize optimize device characteristics. A dual step process will be shown to provide optimal integration of the technology.

Challenges for Forming NiSi Films

The formation of NiSi has many phases [1] compounding the complexity of its formation, however numerous reports [2-4] agree that the predominant phases are Ni₂Si, NiSi and NiSi₂. The first phase of Ni₂Si is formed in the temperature range of 250 to 300 °C. This step provides the foundation for the formation of the lower resistivity NiSi at a higher temperature, but if the temperature is too high, NiSi₂ will form resulting in an undesirable higher electrical resistivity. As shown in the film formation profile of Fig. 1, there are three phases of formation; the lower temperature phase, primarily through nickel diffusion, up to 300 °C when Ni₂Si is formed. This nickel rich formation goes through a rapid transition around 300 °C with the formation of the low resistivity NiSi film. At higher temperatures, as may be used for subsequent fabrication processes, the NiSi₂ high resistivity phase forms thus constraining process window.

In typical processes with 10 nm thick Ni films, the metal film is completely consumed resulting in a film thickness determined by the deposited metal thickness. The formation process relies on Ni diffusion into adjacent silicon, but Ni deposited on top of SiO₂ isolation areas is not consumed but migrates toward poly lines and source/drain silicon regions as shown in Fig. 2. For small geometry devices, Ni diffuses towards the gate poly forming thicker NiSi films at the poly edges [6]. This excessive silicide can be limited by using a dual annealing step where the excess nickel is etched between steps.

A dual step process has been developed with the first step limiting Ni conversion to the intermediate phase of Ni₂Si. One consequence of this reaction is the resistivity non-

uniformity will be higher as shown in Fig. 1, however rectified by a second uniform anneal.

The effects of dopants and their presence in the underlying silicon need consideration[7]. High concentrations of dopants exist in the source/drain and during silicide formation; the dopants accumulate at the silicide/silicon interface as shown in Fig. 3 which lowers the contact resistance [8]. Dopant concentrations increase by a factor of 2 when a single step formation process is used [8]. When NiSi is formed on As doped Si, the resistivity continues increasing with longer annealing, whereas with B doped Si, the resistivity tends to saturate. Ge amorphization is used to enhance boron implantation and found to accelerate the reaction of NiSi formation.

The thermal stability of NiSi limits its use and as noted in Fig. 1, the resistivity remains nearly constant in the temperature range of 320 °C to 550 °C. At temperatures around 550 °C, the agglomeration of the NiSi Films appears as in Fig. 5 and increases resistivity by ratios greater than 2[9]. At temperatures exceeding 750 °C, the high resistivity silicon rich phase of NiSi₂ forms and further agglomerates [10] .

The film degradation as observed through the increase in resistivity has provided insight on the evolution of the film transition. The activation energy for agglomeration is typically ~ 2.4 eV [11] whereas the NiSi to NiSi₂ transformation requires more energy, so NiSi agglomeration occurs prior to forming NiSi₂. Analysis of films formed on As-doped silicon, shows agglomeration forming islands protruding into the silicon surface[12] and were attributed to higher NiSi₂ surface energy compared to the Si surface or NiSi₂/Si interface.[11]. The addition of up to 5 atomic percent Pt to the deposited film overcomes agglomeration through the suppression of NiSi₂ nucleation improving the thermal

stability [13] A high dose implant of BF_2^+ is found to retard the formation of NiSi_2 through F segregation at the interface and grain boundaries [14].

During silicidation, lateral NiSi film growth takes place which is not desirable for maintaining device dimensional control [15]. For the initial Ni_2Si formation step a lower temperature is utilized then by etching the excess nickel the supply of nickel is depleted thus minimizing lateral diffusion. The second higher temperature annealing step transitions the Ni_2Si to low resistivity NiSi [16].

The use of NiSi reduces silicon consumption by nearly 35% for the compared to CoSi_2 allowing smaller dimension design rules and reducing the residual stress in the device structures. Most important, the lower depth penetration means the nickel rich conductor is farther away from the physical junction, thus providing a more defect free junction resulting in lower leakage current [17].

Numerous studies [17] of leakage current in N+/P and P+/N diodes using NiSi have shown that the leakage current is significantly reduced relative to CoSi_2 . The shallowest junctions are the most sensitive to the silicide thickness, however there is less variation with B than with the As doped junctions.

Leakage current has been attributed to the NiSi/Si interface roughness of the formed NiSi film, however the surface is smoother than the Si/silicide interface [12]. The correlation of the roughness to the observed leakage current may be attributed to the formation of pores due to the Kirkendall effect [12]. To further minimize leakage current the Ni needs to be kept from diffusing through the gate electrodes.

The high diffusivity of Ni during the formation processes causes the more narrow lines to form a thicker nickel layer as the nickel is “absorbed” into the poly silicon gate

electrode. This results in a slightly lower sheet resistivity for such narrow lines, referred to as the “reverse linewidth effect”[17]. Again, the dual step process offers a means for minimizing the diffusion while excess Ni is available. However, for NiSi “metal” gates, the available Ni has to diffuse throughout the entire gate electrode region [18].

The formation of electrical contact to source/drain introduces defects formed by the NiSi. Analysis through the use of Deep Level Transient Spectroscopy (DLTS) in the contact region [19] has shown two electron trap levels and one hole trap level are present. The electron trap levels are at $E_c-0.42$ eV and $E_c-0.50$ eV, with the hole trap level at $E_v+0.22$ eV with concentrations of $1E13$ to $1E15/cm^3$.

Native oxides have been known to inhibit or delay silicidation thus requiring higher temperatures or more time. Several studies have shown native oxide to be a stable diffusion barrier to Ni and that the oxide barrier may physically break up during silicidation [20]. The native oxide will suppress NiSi silicidation up to 650 °C [21] requiring higher temperatures to form the silicide. As a cap material, Ti is capable of gettering oxygen within the metal and reducing interfacial oxide to reduce suppression of silicidation. In addition, the Ti cap results in better uniformity, thermal stability [22] and lower junction leakage. TiN has also been used as a cap layer to prevent oxygen diffusion to the Ni/Si interface [23]. The use of TiN also enhances the NiSi formation uniformity, lowers surface roughness and interface roughness and is being used for fully silicided gate electrodes [24].

Device Electrical Performance Review

The leakage currents associated with NiSi contacts [25], in spite of the Ni related electrically active defects, in a majority of diodes have good I-V characteristics with an

ideality factor in the range of 1.01 to 1.08 and saturation currents of $2\text{E}-15$ to $9\text{E}-15$ A. Poor diodes have an ideality factor in the 1.11 to 1.13 range and saturation currents of $5\text{E}-14$ to $3\text{E}-13$ A. Low temperature measurements indicate the “poor” diodes have current flowing through localized Schottky contact areas. The reverse bias current flow shows the presence of very small radii Schottky contacts possibly made by a number of silicide spikes. Such spikes result in electric fields large enough to explain the dominant leakage current due to tunneling. The addition of a small amount of Pt to the Ni improves the integrity of the junctions [26].

Excess silicidation occurs in small diode regions and results in higher leakage currents and poly depletion. To minimize excess silicide formation, a lower Ni_2Si formation temperature is needed when Ni is abundantly available.

Extending the use of NiSi even further, the fabrication of fully depleted devices and their associated benefits is realizable [27]. It has been shown that the mobility is high and reverse breakdown characteristics are comparable to poly gates. These devices employ a poly gate where the NiSi penetrates through the entire gate electrode forming a NiSi gate. The process steps for fabrication are more complex as outlined in the reference [27] and the key parameters for formation of the silicide are the Ni film thickness control and low temperature process.

During the formation of NiSi, Ni residing on the isolation regions will react with the oxide or nitride. The etching step after the initial phase formation does not remove all the residual Ni due to the reaction between the Ni and underlying dielectric layer. The reaction can be minimized by using a low temperature, less than $350\text{ }^\circ\text{C}$, for forming the Ni_2Si phase.

Experimental Data and Discussion

Experiments utilizing the following process sequence were performed to determine the optimum conditions to form the Ni₂Si phase primarily focusing on low silicon consumption, yet achieving a low sheet resistivity. The three step process consists of:

1. Initial low temperature anneal at 260 to 300 C for forming Ni₂Si
2. Etching the excess Nickel with selective wet etching solution
3. Higher temperature anneal, 400 to 450 C for forming a stable film of NiSi

The WaferMasters' Stacked Annealing Furnace (SAF) was used for the experiments with the system configuration consisting of 5 isothermal cavities as shown in Fig. 6. Wafers are placed midway between the heating plates resulting in equal heating from both sides of the wafer for good temperature uniformity to minimize stress. The resistance based furnace eliminates the effects of emissivity and reflectivity and provides a uniform temperature environment for the wafer.

The first annealing step is performed in the temperature range of 300 to 320 °C for a typical 10 nm thick Ni film covered by 10 nm of TiN. The data of Fig. 7 shows the nickel transformation to the Ni₂Si phase and eventually at higher temperatures to NiSi. The processing period of 300 seconds, from initial placement of the wafer in the isothermal cavity to removal, NiSi formation is at about 300 °C. A more precise transformation temperature can be derived from measurement of the R_s non-uniformity as shown in Fig. 8 where the phase change takes place at 310 °C. With varying nickel film thickness and capping films, the transformation temperature can be shifted.

To evaluate the sensitivity of the final NiSi film based on the first anneal, a set second anneal was performed at 450 °C for 300 seconds. This provides an indication of how Ni₂Si is formed and how it affects the formation of the desired film NiSi. With the data shown in Fig. 9, enough Ni₂Si is formed at lower temperatures, as low as 270 °C, to achieve a low resistivity NiSi film. This information can then be used to reduce the thermal budget requirements for forming NiSi films.

Experiments were performed with N+/P diodes to evaluate leakage current characteristics of various NiSi formation processes. The initial tests were performed with the “standard” single cycle annealing at 450 °C for 5 minutes with the resulting leakage shown in Fig. 10. The temperature was lowered to 400 °C and found to improve the leakage, however the resistivity was slightly higher. Subsequent processing was performed with the dual step process at the indicated temperatures for the initial and post Ni etch step. All the dual step anneals showed improved leakage characteristics and low film resistivity as seen in recent reports, [28].

Conclusions

To enable the implementation of NiSi for sub 65 nanometer technology, a two-step annealing process has been shown to resolve many of the limitations in using NiSi. Starting with limiting silicon consumption to minimizing defect generation, the two-step sequence provides the means for achieving stable NiSi films with a reduced thermal budget. Utilizing a resistive heated based annealing system, the uniform heating of the wafer minimizes the stress of the formed NiSi film which reduces electrical leakage.

Through varying the second anneal step, the initial formation of Ni₂Si can be performed at lower temperatures reducing the thermal budget and silicon consumption. A

lower initial temperature anneal also reduces lateral diffusion of Ni, a source of defect generation.

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List of Figure Captions

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- Figure [2](#). Illustration of Ni migration to poly line, causing elevated poly edges
- Figure [3](#). Dopant pile-up at the diffusing NiSi interface.

Figure [4](#). Agglomeration of NiSi at temperatures exceeding 550 °C.

Figure [5](#). Stacked annealing furnace configuration with 5 isothermal cavities.

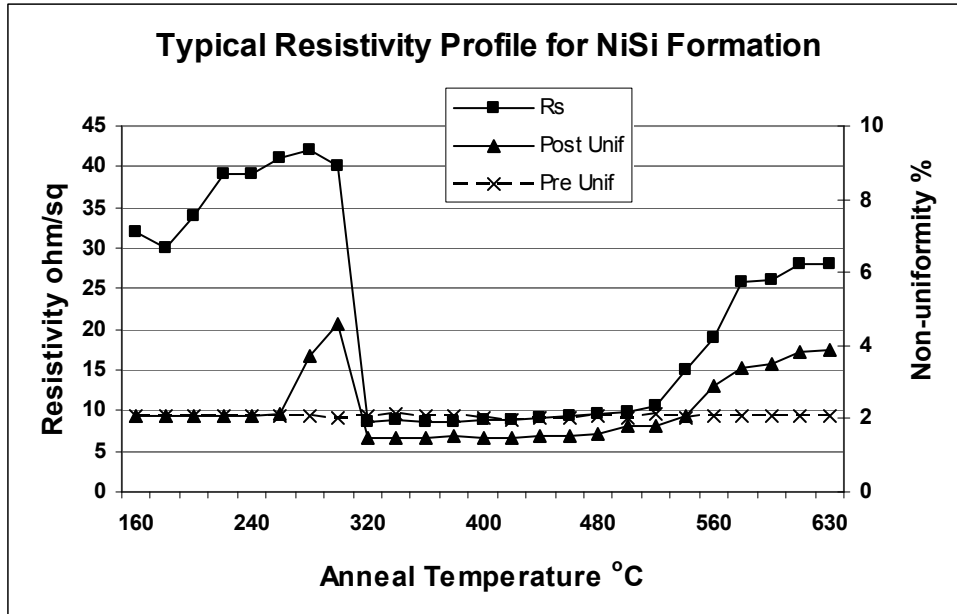
Figure [6](#). Ni₂Si transformation with RTA1, initial anneal cycle

Figure [7](#). Sheet resistivity non-uniformity resulting from initial anneal cycle, RTA1

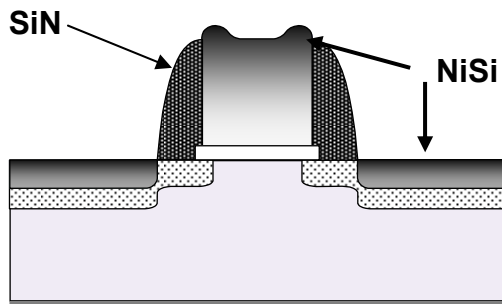
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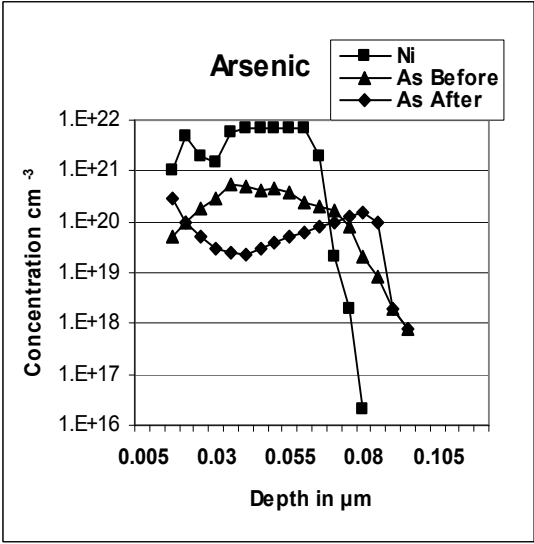
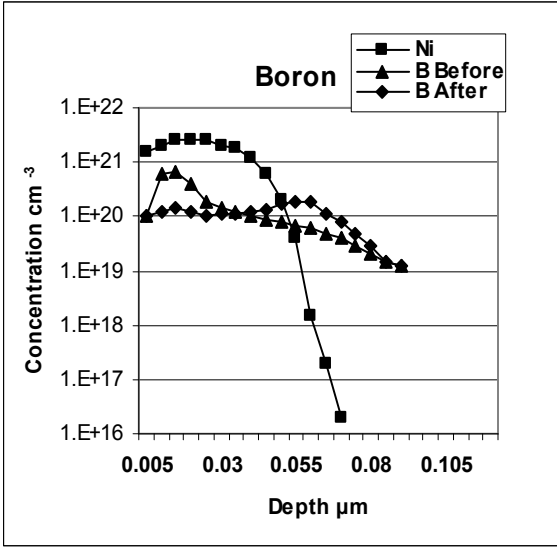
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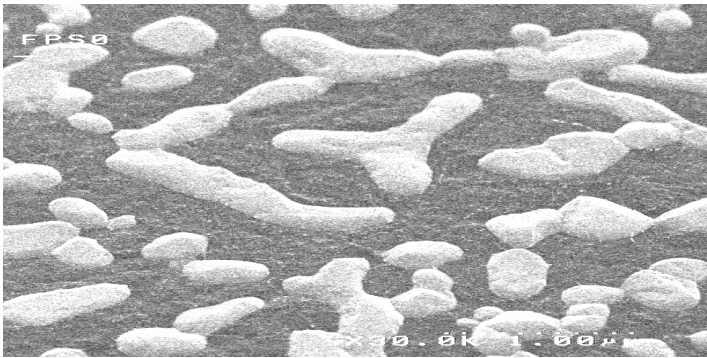
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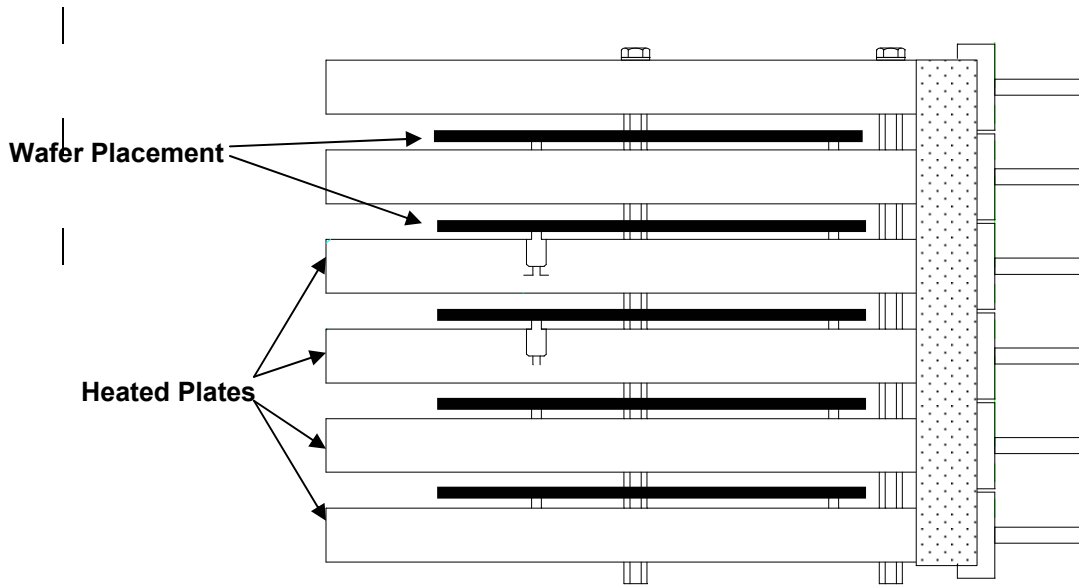
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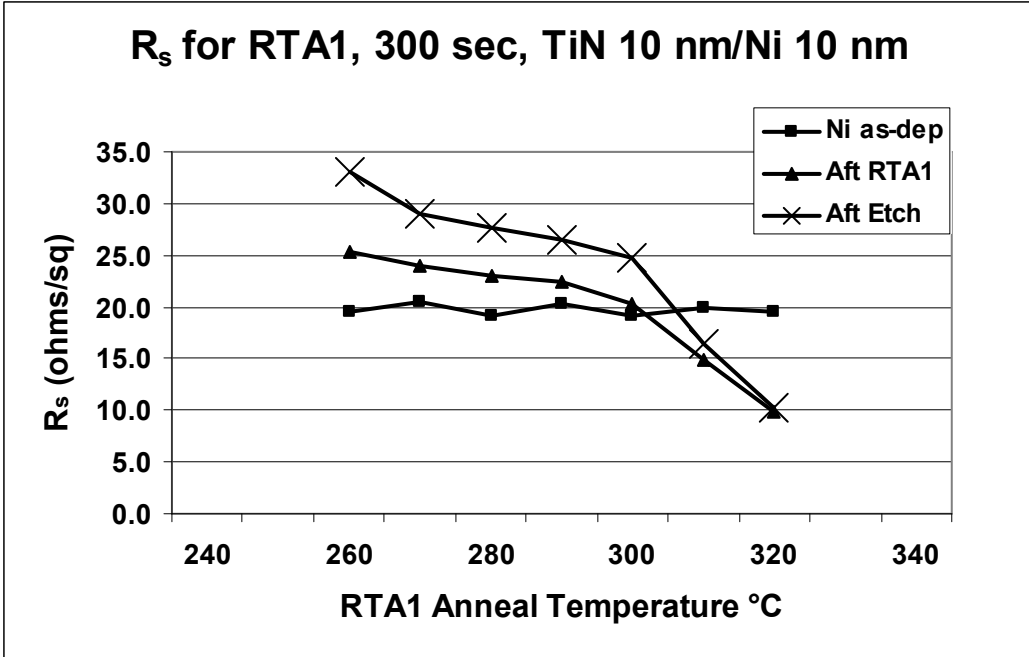
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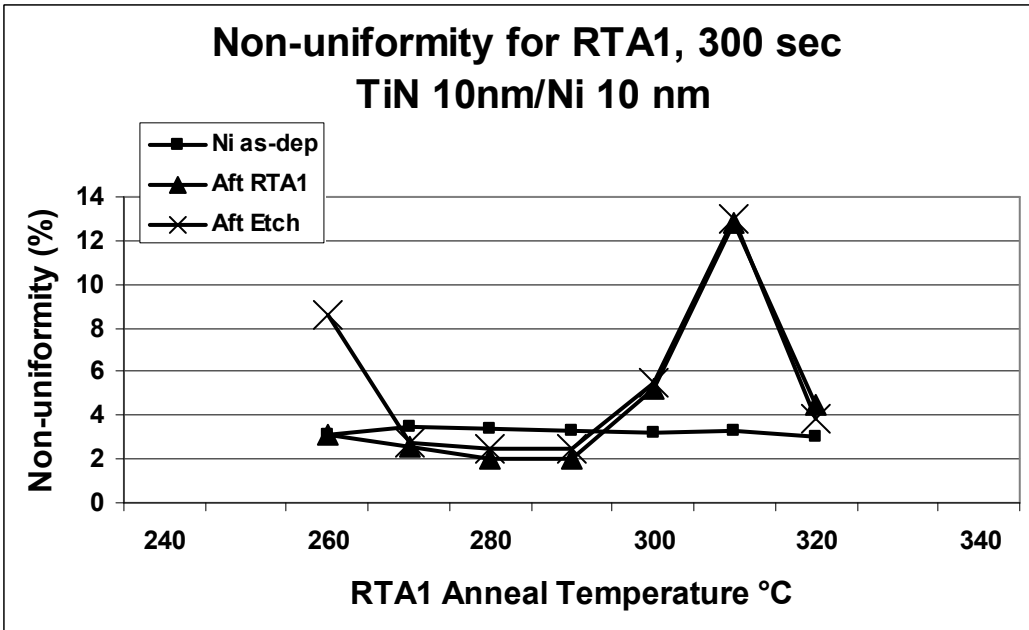
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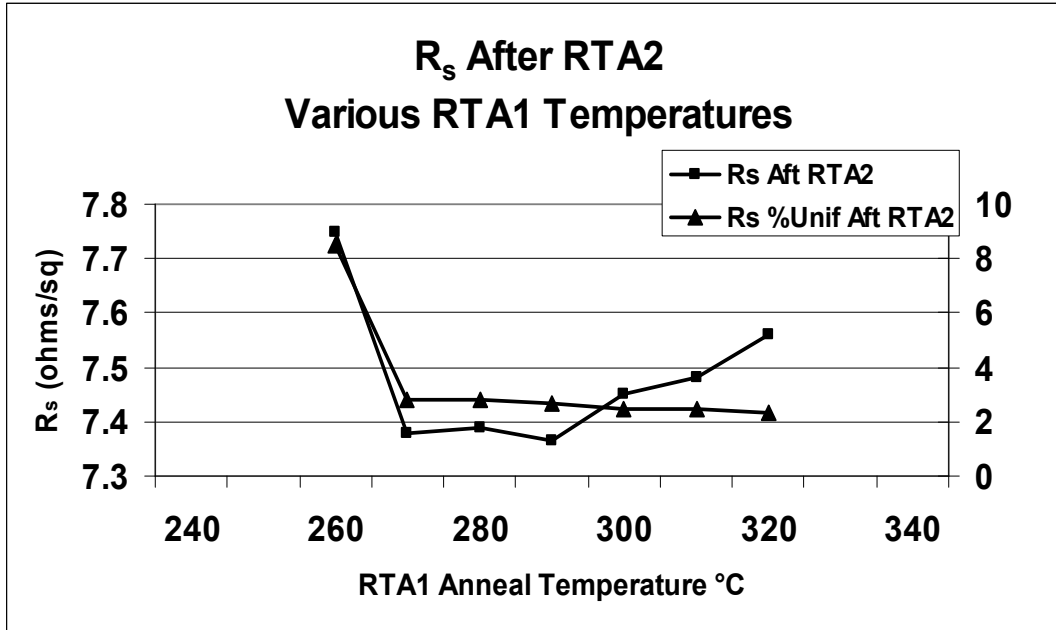
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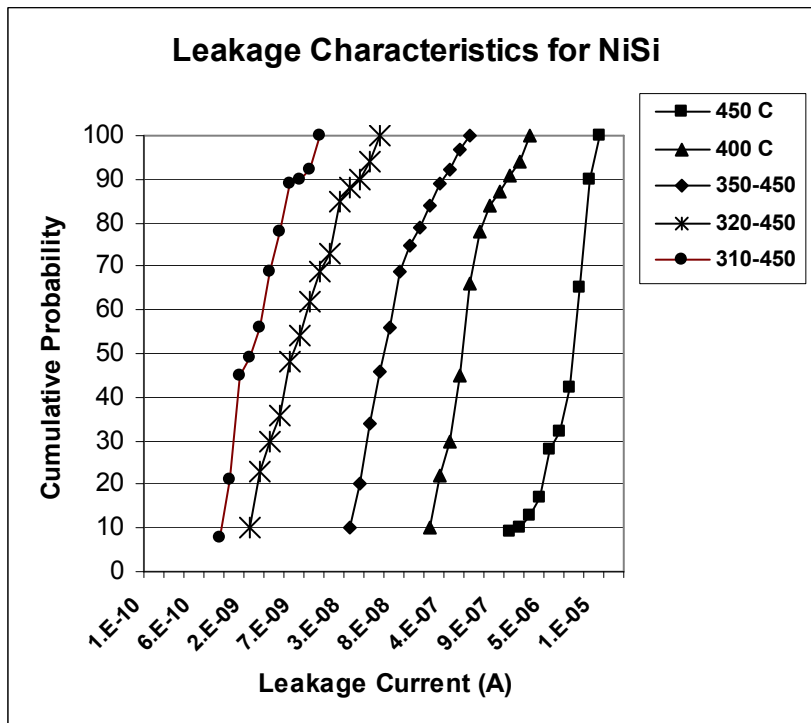
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