Post-Anneal Stress Reduction of 200 mm Silicon Wafers in Single Wafer Rapid Thermal Annealing

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ABSTRACT

In every wafer processing step wafer stress management is extremely important for advanced device manufacturing. Thermally induced stress on device wafers has a large impact on lithography and affects device yield. Thermally induced stress during rapid thermal annealing (RTA) steps in high density 512MB DRAM device fabrication was investigated using a lamp-based (cold wall) RTA system and compared to results using a furnace-based (hot wall) single wafer RTA system. Compared to the lamp-based (cold wall) system, RTA in a furnace-based (hot wall) system was found to be very effective in suppressing thermally induced stress and increasing device yield due to superior pattern transfer characteristics in lithography.

INTRODUCTION

Minimizing the variation in device performance (within wafer and wafer-to-wafer) is very important for device yield management and quality control. For advanced ultra large scale integrated circuit (ULSI) devices, with design rules below 130 nm, the precise control of thermal budget is one of the key issues in thermal processing to optimize device performance. With the shrinkage in device dimensions and allowable thermal budgets, lamp-based single wafer rapid thermal annealing (RTA) systems became very popular addressing thermal processing applications. However, thermally induced stress in wafers during RTA processes can cause small distortions to the wafer surface, which increases the difficulty of subsequent lithography steps.

In a lamp-based RTA system (cold wall system) with multiple zone temperature control, the temperature of an individual zone is dynamically controlled using feedback signals from in-situ pyrometric temperature measurements of the zones on the wafer. Precise wafer temperature control and measurement are a technical challenge, as lamp power is constantly modulated by the feedback signals from the wafer temperature monitoring zones. In the dynamic wafer temperature control mode used in the lamp-based RTA systems, it is difficult to maintain temperature uniformity during the process. Local and global temperature repeatability depends on many factors, such as the emissivity distribution of the wafer, chamber wall temperature and chamber wall reflectivity. Frequent calibration and maintenance are required. It is well known that RTA processes using conventional lamp-based RTA system generate localized hot and cold spots due to the difference in absorption and emission characteristics within wafers, especially on patterned wafers [1, 2]. Thermally induced stress during RTA processes causes local and global distortions to the wafer surface. As a result, control of the subsequent lithography steps becomes very difficult. The small distortions induced by the

RTA process steps are no longer negligible in achieving the resolution requirements of lithography for advanced ULSI devices.

In this paper, the authors performed a comparative study of several critical RTA annealing process steps to investigate post-anneal wafer stress in wafers annealed using a lamp-based (cold wall) RTA system and a furnace-based (hot wall) SRTF system. The lamp-based RTA system controls the wafer temperature based on a programmed temperature profile by controlling the power to the lamps whereas the furnace-based RTA system processes a wafer in a preheated furnace (chamber) by controlling wafer residence time in the heated chamber. Stress of various types of wafers was measured before and after RTA under various annealing conditions.

EXPERIMENTAL DETAILS

To investigate the post-anneal stress in wafers, a comparative study of several critical RTA process steps was performed using a dual bank lamp-based (cold wall) RTA system and a furnace-based (hot wall) single wafer rapid thermal furnace (SRTF) system. Details of the SRTF system used for this study is reported elsewhere [3 - 5]. Stress on various types of wafers was measured before and after RTA under various annealing conditions in the temperature range of 1000~1100°C using both types of RTA systems. The effect of annealing temperature and the heat transfer mechanism of both system types on oxygen (Oi) concentration in silicon was investigated. Wafers with three different Oi concentrations (low: ~1.1×10^{18} cm^{-3}, medium: ~1.25×10^{18} cm^{-3} and high: >1.3×10^{18} cm^{-3}) were evaluated. In addition, wafers having an epilayer and poly back seal (PBS) layer were compared. The wafer warpage before and after annealing was measured. The wafer warpage before annealing varies between 10~30 μm depending on the Oi concentration and additional film stacks. The measured average wafer warpage is summarized in Table 1.

Table 1. Average wafer warpage before annealing.

Oi Conc.	Wafer Type			
	Blanket	With PBS layer	With epilayer	With PBS and epilayer
Low	~10 μm	~30 μm	~15 μm	~30 μm
Medium	~10 μm	~20 μm	~15 μm	~20 μm
High	~15 μm	~20 μm	~10 μm	~20 μm

Prior to the wafer warpage investigation, the temperature of the lamp-based RTA system and hot wall RTA system was calibrated utilizing the measurement of oxide growth rate and implant activation. The process uniformity of both systems was maintained at 1σ below 1%. In this study, the wafer temperature ramp rate and process time at the annealing temperature were fixed at 55°C/s and 10 s, respectively.

Figure 1 shows contour maps of the optical interference measured on wafers annealed by the dual bank lamp-based RTA system at 1000°C. The number below each contour map indicates wafer warpage. In the case of wafers without an epilayer, wafer warpage after RTA becomes larger as the oxygen concentration increases. The greater the wafer warpage, the more difficult mask alignment becomes during photolithography. The incremental increases in thermally induced wafer warpage during RTA makes subsequent lithography extremely difficult and has a strong impact on device yield in advanced devices with small feature sizes especially below 110 nm.

Wafers with an epilayer showed significantly less warpage after the lamp-based RTA at 1000°C compared to the ones without the epilayer, as shown in Figure 2. Furthermore, the wafers with an epilayer did not show thermally induced wafer warpage with respect to increases in oxygen concentration. Beside the more optimal characteristics achieved with RTA, wafers with an epilayer have higher crystalline quality and electrical properties. Wafers with an epilayer are more suitable for device fabrication from the process quality control point of view. Wafer warpage after annealing at 1000°C using the lamp-based RTA system is summarized in Fig. 3.

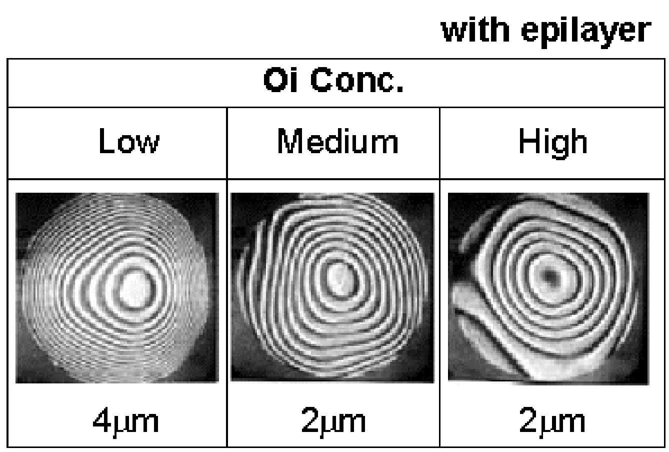

Fig. 1. Contour maps of optical interference measured on wafers without an epilayer annealed by a lamp-based RTA system at 1000°C.

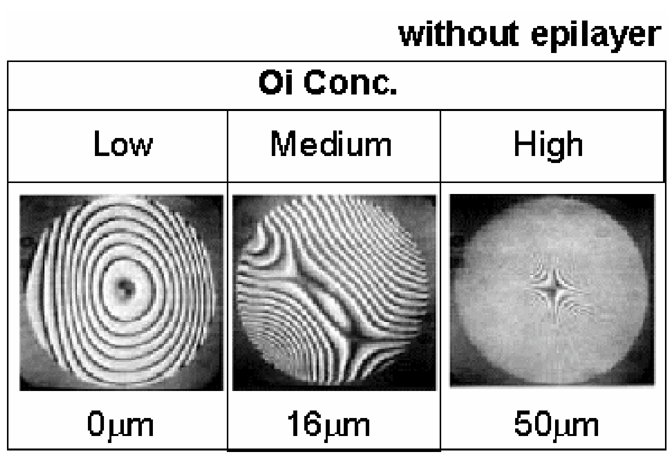

Fig. 2. Contour maps of optical interference measured on wafers with an epilayer annealed by a lamp-based RTA system at 1000°C.

High Oi concentration wafers with and without epilayer were annealed at 1100°C using the lamp-based RTA system to investigate the effect of annealing temperature, Oi concentration and PBS layer on wafer warpage. Figure 4 summarizes the wafer warpage after annealing. Wafers without an epilayer showed a significant increase (>50%) of wafer warpage after RTA. No significant change in warpage was observed from wafers with the epilayer. The wafers with the epilayer were reasonably flat before and after annealing at 1000°C or 1100°C using the lamp-based RTA system. It appears that lamp-based systems have reduced wafer warpage when using wafers having epilayer. In a mass production environment, material cost is one of the most important factors to be considered. If one can use lower cost wafers without an epilayer, instead of expensive wafers with an epilayer, it would have significant economic impact.

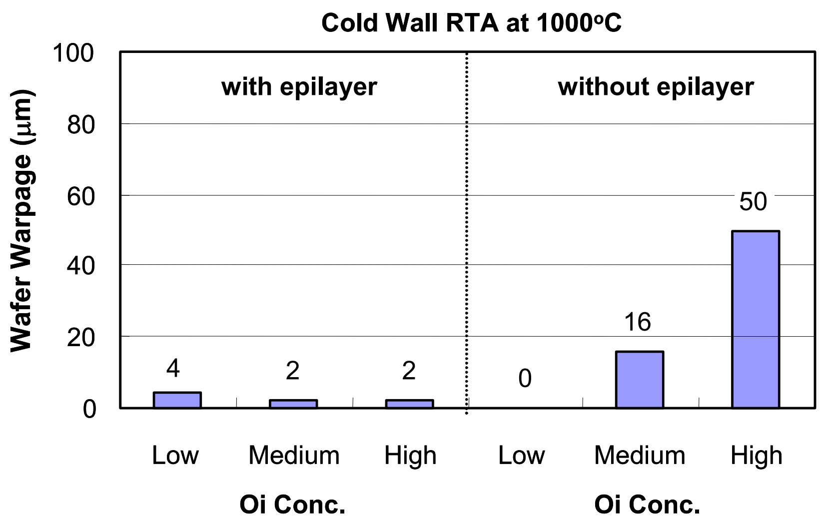

Fig. 3. Effect of epilayer and Oi concentration on wafer warpage after annealing at 1000°C using a lamp-based RTA system.

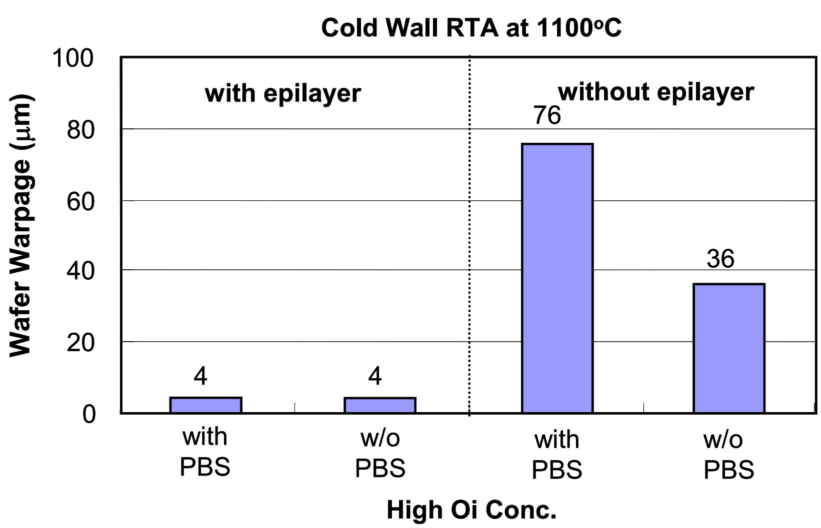

Fig. 4. Effect of epilayer and PBS layer on wafer warpage in wafers with high Oi concentration after annealing at 1100°C using a lamp-based RTA system.

To investigate the effect of the heat transfer mechanism in the annealing system on thermally induced wafer warpage, the same series of experiments performed on the lamp-based system was repeated using the furnace-based, hot wall SRTF system. General trends were the same as the experimental results achieved using the lamp-based RTA system. Wafers with an epilayer showed much less warpage compared to those without the epilayer after the furnace-based RTA, regardless of annealing temperature and oxygen concentration (Oi) in Si. In addition, wafers without an epilayer and annealed using the furnace-based SRTF system showed much less thermally induced stress, including warpage, compared to those wafers annealed using the lamp-based RTA system. As shown in Fig. 5, the high Oi concentration wafers annealed at 1000°C using the SRTF system showed 25 times less thermally induced warpage (2 μm versus 50 μm) than the same type of wafers annealed using the lamp-based RTA system. The medium Oi concentration wafers annealed at 1100°C using the SRTF system also showed ~3 times less thermally induced warpage (22 μm versus 64 μm) than the same type of wafers annealed using the lamp-based RTA system. Significant reduction of thermally induced stress on wafers annealed above 1000°C was achieved by annealing in the hot wall RTA system with very repeatable results. Figure 5 summarizes the wafer warpage comparison after annealing at 1000°C and 1100°C using the lamp-based RTA system and the furnace-based SRTF system. The effect of a poly back seal (PBS) layer on thermally induced stress was also investigated using both types of RTA systems. The wafers with a PBS layer show a slight reduction of thermally induced stress after RTA when using the hot wall system.

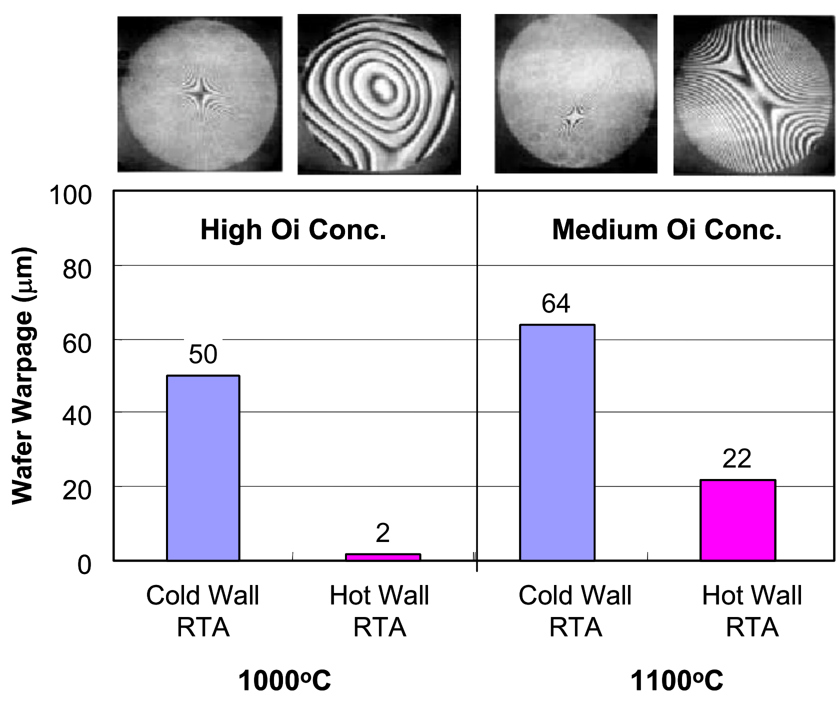

Fig. 5. Wafer warpage comparison after annealing at 1000°C and 1100°C using a lamp-based RTA system and a furnace-based SRTF system.

DISCUSSION

A cross sectional TEM (transmission electron microscopy) study of annealed wafers showed very clear correlation between the thermally induced stress and oxygen precipitate levels in Si. The higher Oi concentration and local temperature non-uniformity during high temperature RTA enhance oxygen precipitation in Si. During the cool down process, the thermally induced stress becomes fixed. Defects in silicon crystals and their impact on DRAM device characteristics were throughly investigated in detail by Dornberger *et al*. [6]. In lamp-based RTA systems, arrays of tungsten halogen lamps are used as the heat source. Global temperature uniformity on the wafer is achieved by dynamic power control of the lamp(s). At the microscopic level, many hot and cold spots are generated on patterned wafers during RTA due to optical interaction between radiation from the array of lamps and the patterned wafer [1, 2]. The lamp-based RTA systems rely entirely on radiation heat transfer and must account for variations in emissivity dependency and patterned material reflectivity. To achieve similar process results, regardless of film structure and/or pattern density, the lamp power has to be dynamically controlled based on the backside emissivity dependent wafer temperature measurement values which can be a source of inaccuracy. Conversely, the furnace-based SRTF system provides a nearly isothermal processing environment by employing a stable, heated cavity surrounding the wafer, regardless of film structure and/or pattern density [3 - 5]. The surrounding planar heat source (heated cavity) provides uniform heat to the wafers through all three heat transfer mechanisms (conduction, convection and radiation). The process results show significantly less dependency on emissivity and/or pattern density, thus are extremely repeatable. In the case of wafers with an epilayer, most of the oxygen was driven out during high temperature epitaxial growth at approximately $1100^{o}C$ and so the oxygen concentration is already reduced prior to the RTA step. Thus, wafers with an epilayer are less sensitive to the RTA processing environment. By switching the RTA method from cold-wall to hot-wall processing, thermally induced stress after RTA is minimized, which benefits subsequent lithography steps. Low cost wafers (without an epilayer) can be used as product wafers without the limiting photolithography processing due to warpage.

In mass production of 512MB DRAM devices with 110nm design rules, significant improvement in electrical characteristics and post-anneal wafer stress was achieved by utilizing annealing from the furnace-based SRTF system. Besides wafer warpage, the standard deviation of p- and n-channel resistance values of devices within the wafer and wafer-to-wafer, was 2 to 3 times smaller than that from wafers annealed using the lamp-based RTA systems. Emissivity dependence and pattern density effects were also negligible in the furnace-based SRTF system [3 - 5]. The detailed comparison of electrical performance of 512MB DRAM devices fabricated using the lamp-based RTA system and the furnace-based SRTF system was reported elsewhere [7]. By employing the furnace-based SRTF system for the RTA steps, thermally induced wafer warpage was significantly reduced and the electrical performance of devices showed smaller deviation. The hot wall RTA system is very well suited for thermal processing of advanced devices.

SUMMARY

A comparative RTA study was performed in the temperature range of $1000\sim1100^{o}C$ using a lamp-based (cold wall) RTA system versus a furnace-based (hot wall) SRTF system. Stress or warpage of various types of wafers was measured before and after RTA under various annealing conditions. Wafers with an epilayer were relatively flat before and after RTA steps regardless of annealing temperature RTA system. Wafers without an epilayer, however, showed significant wafer warpage after annealing above 1000^{o}C in the cold wall RTA system. In contrast, wafers without an epilayer did not show a wafer warpage increase even after annealing above 1000^{o}C in the hot wall RTA system. The effect of Oi concentration on wafer warpage increase after annealing in the hot wall RTA system was negligible. Even after a 1100^{o}C annealing, only a slight increase of warpage from ~15 μm to 22 μm was observed in a wafer with high Oi concentration. The flatness of wafers after annealing in the SRTF system was significantly improved (up to ~25 times) compared to those annealed using the lamp-based RTP systems. The "nearly" isothermal process environment of the SRTF system made subsequent lithography steps easier regardless of wafer type by reducing thermally induced stress causing warpage.

In mass production of 512MB DRAM devices with <130 nm design rules, significant improvement in electrical characteristics and post-anneal wafer stress was achieved by using the furnace-based SRTF system as compared to ones annealed by the lamp-based RTA system. The standard deviation of p- and n-channel resistance values of devices within wafer and wafer-to-wafer, was reduced by 2 to 3 times compared to wafers annealed using the lamp-based RTA systems. Emissivity dependence and pattern density effects on wafers annealed in SRTF system are negligible compared to the lamp-based RTA systems. Expensive epi wafers can be replaced with non-epi wafers in advanced DRAM manufacturing by using the hot wall based RTA system. This has a very significant technical and economic impact on device manufacturing.

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