

Rapid Thermal Annealing of Arsenic Implanted Silicon Wafers

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Abstract

Rapid thermal annealing of ⁷⁵As⁺ implanted Si wafer (200mm in diameter) was done using a lamp-based RTP system and a single wafer rapid thermal furnace system under 1 atm N₂ atmosphere to mainly understand electrical activation and dopant diffusion phenomena. The implant energy and doses were varied in the range of 3keV~70keV and 1x10¹⁵~1x10¹⁶ atoms/cm², respectively. Average sheet resistance and its uniformity of ⁷⁵As⁺ implanted wafers were measured after annealing. Arsenic depth profiles were investigated using the secondary ion mass spectroscopy.

Introduction

In recent years, rapid thermal annealing (RTA) has become the preferred method implant annealing method. Annealing temperature, wafer temperature ramp up/down rate, annealing time and process atmosphere are varied to optimize annealing conditions. Measured sheet resistance and its uniformity values after annealing are frequently used for optimizing annealing conditions. As device dimensions shrink, the formation of shallow junction becomes very important.

A very short time annealing at higher temperature with a very fast ramp up/down rate ("spike anneal") has been introduced as an effective implant annealing method to electrically activate implant species with the least amount of diffusion during the annealing process [1-2]. The process window of the spike anneal is very narrow because it strongly relies on temperature measurement/control accuracy in a wide temperature range (room temperature ~1150°C) during a very short period of annealing time (<1s). For the successful formation of shallow junctions in mass device production environment, a wide annealing process window for a low sheet resistance and an abrupt dopant

profiles is required. Fundamental understanding of damage recovery, electrical activation and dopant diffusion during implant anneal is necessary to establish production-worthy processes.

In this study, RTA of ⁷⁵As⁺ implanted Si wafer (200mm in diameter) with various implant energies and doses was done using a lamp-based rapid thermal processing (RTP) system and a single wafer rapid thermal furnace (SRTF) system under 1 atm N₂ atmosphere to mainly understand electrical activation and dopant diffusion phenomena.

Experiment

A. Lamp-based RTP System

The lamp-based RTP system used in this study employs banks of linear tungsten halogen lamp array and illuminate a Si wafer from top and bottom sides through the quartz process tube. Wafer temperatures are measured using a pyrometer through the quartz tube. Multiple zone power control method is used to adjust temperature uniformity on a Si wafer. Wafer temperature ramp up rate, soak time and ramp down rate are programmable.

B. SRTF System

A dual chamber SRTF system with a vacuum loadlock was used in this study. The process tube is made of clear quartz and has three quartz standoffs. The process tube uses no moving parts for simplicity and system reliability. The wafer is placed on the quartz standoffs (8~9mm tall) in the middle of quartz process tube. The distance between the wafer and the quartz walls is kept at ~10mm for both upward and downward directions. The quartz process tube is located in a SiC cavity which acts as heat distributor to create isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly.

The temperature of the SiC cavity is monitored and controlled at a predetermined process temperature by three embedded R-type thermocouples and the three zone heater assembly. Detailed configuration, thermal characteristics and process performance of the system has been reported elsewhere. [3]

C. Implant Anneal

Implant wafers were annealed using the lamp-based RTP system and SRTF system in mass production environment. The implant energy and doses were varied in the range of 3keV~70keV and $1 \times 10^{15} \sim 1 \times 10^{16}$ atoms/cm², respectively. 200mm diameter Si wafers implanted with various species were annealed using the lamp-based RTP system and SRTF system under 1 atm N₂ atmosphere to compare resulting average sheet resistance and its uniformity after annealing. The annealing temperature was varied between 900°C and 1100°C. Fig. 1 shows typical wafer temperature profiles during annealing process at 1000°C. Process time (wafer residence time in furnace) for the SRTF system in the temperature range of 900°C~1100°C can be easily estimated by simply adding 30s to the “soak time” in the lamp-based RTP system because it is approximately equal to “ramp up time” plus “soak time” in the lamp-based RTP system. Average sheet resistance measurement after implant anneal at 1000°C using the SRTF system and lamp-based RTP system indicated that the estimated process time for the SRTF system (30s addition to the “soak time” in the lamp-based RTP system) gives equivalent average sheet resistance after annealing.

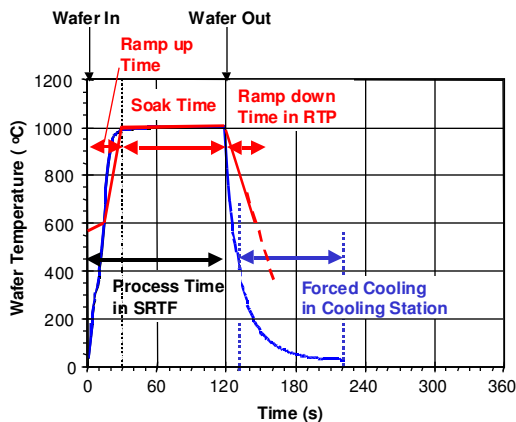


Fig. 1. Typical wafer temperature profiles during 90s process in lamp-based RTP system and 120s process in SRTF system.

The annealing time for the lamp-based RTP system was varied between 10s and 150s. The annealing time for the SRTF system was varied between 40s and 180s.

D. Characterization

The sheet resistance of annealed wafers were measured at 49 points using a four-point probe. 5mm edge exclusion was used during the sheet resistance measurement. Surface response of average sheet resistance and its uniformity were used for process window determination. Dopant depth profiles were also measured before and after annealing using a secondary ion mass spectroscopy (SIMS) to investigate dopant diffusion during annealing.

Results and Discussion

Surface response of average sheet resistance of ⁷⁵As⁺ implanted wafers (70keV, 1×10^{15} atoms/cm²) after annealing using a lamp-based RTP system is plotted in Fig. 2. A contour line of average sheet resistance uniformity at 0.5% (1σ) is also plotted in Fig. 2. Process window is indicated as shaded area. Average sheet resistance $\rho_s < 92(\Omega/\text{sq.})$ and its uniformity $< 0.5\%(1\sigma)$ were used for process window determination criteria. The average sheet resistance value decreases as annealing temperature increase and annealing time increase in the temperature range of 900°C~1000°C. A contrary trend was observed in the temperature range of 1000°C~1100°C. The average sheet resistance value increases as annealing temperature increase and annealing time increase in the temperature range of 1000°C ~1100°C.

Fig. 3 shows the surface response of average sheet resistance of ⁷⁵As⁺ implanted wafers (70keV, 1×10^{15} atoms/cm²) after annealing using the SRTF system. A contour line of average sheet resistance uniformity at 0.5% (1σ) is also plotted in Fig. 3. Similar trends in the average sheet resistance were observed in ⁷⁵As⁺ implanted wafers annealed using a SRTF system. A lower average sheet resistance was obtained in wafers annealed using the SRTF system in the temperature range of 900°C~1050°C. The sheet resistance uniformity of wafers annealed using the SRTF system was always better. As a results of the lower sheet resistance and better sheet resistance uniformity, the process window for the SRTF system found to be almost 4 times larger than that for the lamp-based RTP system.

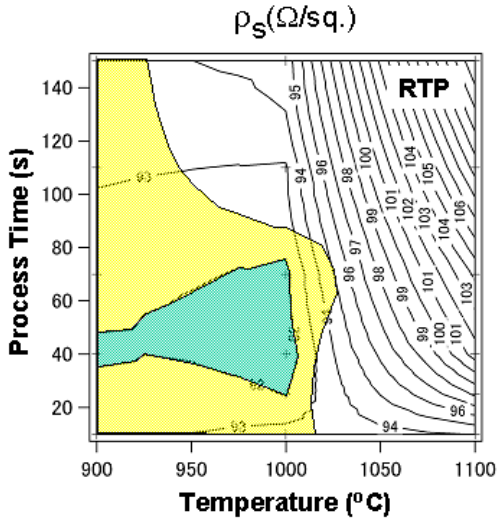


Fig. 2. Surface response of sheet resistance of $^{75}\text{As}^+$ implanted wafers after annealing using lamp-based RTP system. ($^{75}\text{As}^+$ 70keV, 1×10^{15} atoms/ cm^2)

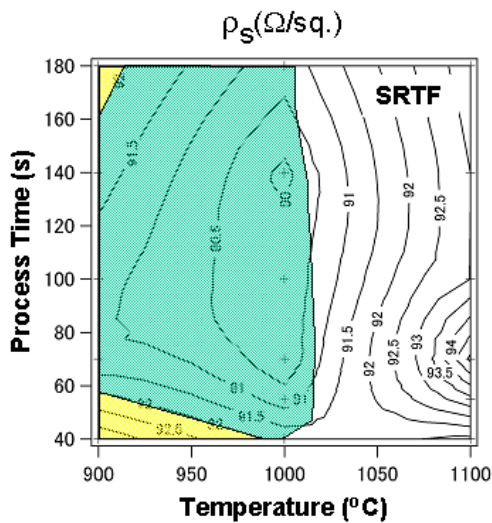


Fig. 3. Surface response of sheet resistance of $^{75}\text{As}^+$ implanted wafers after annealing using SRTF system. ($^{75}\text{As}^+$ 70keV, 1×10^{15} atoms/ cm^2)

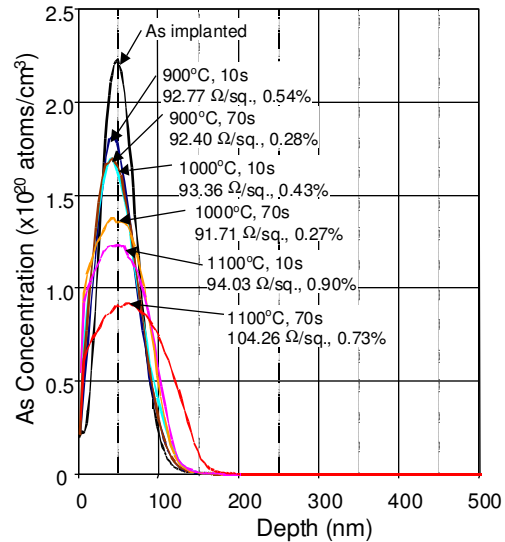
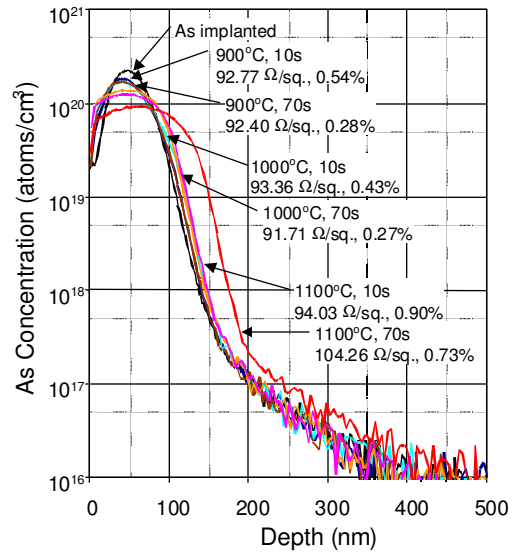


Fig. 4. Semi-logarithmic and linear SIMS depth profiles of $^{75}\text{As}^+$ implanted wafers after annealing using lamp-based RTP system. ($^{75}\text{As}^+$ 70keV, 1×10^{15} atoms/ cm^2)

Fig. 4 show semi-logarithmic and linear SIMS depth profiles of $^{75}\text{As}^+$ implanted wafers (70keV, 1×10^{15} atoms/ cm^2) after annealing using the lamp-based RTP system. The average sheet resistance and its uniformity values were indicated along with individual dopant depth profile. As seen in the figures, dopants diffuse faster at higher temperatures and diffuse more as annealing time increases at a given annealing temperature. The average sheet resistance decreases as dopants electrically activates during RTA. Sufficient electrical activation has been

observed in wafers annealed at 900 $^{\circ}\text{C}$ regardless of annealing system. 70s annealed wafers always showed lower average sheet resistance values compared to 10s annealed wafers at 900 $^{\circ}\text{C}$ and 1000 $^{\circ}\text{C}$. Conversely, the 70s annealed wafer showed higher average sheet resistance value compared to the 10s annealed wafer at 1100 $^{\circ}\text{C}$ using the lamp-based RTP system.

In the initial stage of annealing, dopant nearly symmetrically diffuses both surface and bulk directions and maximum dopant concentration gradually decreases with time. As annealing

proceeds, the dopant profile becomes asymmetrical. The dopant concentration near surface increases initially and decreases due to the one way diffusion into bulk with the increase of annealing time. In wafers annealed at 1100°C using the SRTF system, the maximum dopant concentration was observed at the surface of wafer. The dopant concentration at the surface was always higher in wafers annealed using the SRTF system compared to wafers annealed using the lamp-based RTP system.

The authors believe that the difference in dopant depth profiles between wafers annealed using the lamp-based RTP system and the SRTF system is originated by the difference in wafer heating mechanism. The lamp-based RTP system and SRTF system can be classified as cold wall system and hot wall system, respectively. The lamp-based RTP system uses the internal heating mechanism where as the SRTF system uses the external heating mechanism. At a given wafer temperature, the SRTF system always gives higher surface temperature. The higher surface temperature makes dopant diffusion to the surface easier. From the device fabrication point of view, higher dopant concentration at the wafer surface is desirable to reduce contact resistance.

To date, many reports have been made on a very short time annealing at higher temperature with a very fast ramp up/down rate (“spike anneal”) as an effective implant annealing method to electrically activate implant species with the least amount of diffusion during the annealing process [1-2]. The sheet resistance measurements and SIMS depth profiles of implanted wafers after annealing strongly suggest that longer annealing (significantly longer than the “spike anneal”) at lower temperature would be better to achieve maximum electrical activation with minimum dopant diffusion. Theoretically, the diffusivity of atoms in Si increases exponentially as annealing temperature increases and the increase in diffusion length is proportional to square root of annealing time at a given temperature [4]. The total diffusion length is proportional to the square root of the product of diffusivity and time.

The process window of the “spike anneal” is very narrow because it strongly relies on temperature measurement/control accuracy in a wide temperature range (room temperature ~1150°C) during a very short period of annealing time (<1s). For the successful formation of shallow junctions in mass device production environment, a wide annealing process window

for a low sheet resistance and an abrupt dopant profile is required. For the production-worthy, repeatable process results in the average sheet resistance and sheet resistance uniformity, a reasonable length of annealing time at an optimum (reasonable) temperature is desired rather than a “spike anneal” at maximum temperature.

Other $^{75}\text{As}^+$ implanted wafers (implant energy: 3keV and 20keV, dose: $1 \times 10^{15} \sim 1 \times 10^{16}$ atoms/cm²) also showed similar trends in electrical activation and dopant diffusion. Fundamental understanding of damage recovery, electrical activation and dopant diffusion during implant anneal is necessary to optimize implant annealing process.

Summary

Rapid thermal annealing of $^{75}\text{As}^+$ implanted Si wafer (200mm in diameter) was done using a lamp-based RTP system and a SRTF system under 1 atm N₂ atmosphere to mainly understand electrical activation and dopant diffusion phenomena. The implant energy and doses were varied in the range of 3keV~70keV and $1 \times 10^{15} \sim 1 \times 10^{16}$ atoms/cm², respectively. Average sheet resistance and its uniformity of $^{75}\text{As}^+$ implanted wafers were measured after annealing. SIMS analysis was done for As depth profiling. The SRTF system resulted in equivalent or better electrical activation and smaller dopant redistribution in depth direction compared to the lamp-based RTP system.

References

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