# Electrical Activation of Ultra-Shallow B and $BF_2$ Implanted Silicon by Flash Anneal

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***Abstract-* Ultra-shallow ion implanted Si wafers, both with and without Ge pre-amorphization, were annealed using xenon arc flash lamps. The duration of flash illumination was controlled between 0.1 ms and 10 ms. Changes in sheet resistance and dopant profiles after flash anneal were measured and investigated, along with crystal defect densities. Sheet resistance measured using a four-point probe. Dopant depth profiling and defect characterization were done using secondary ion mass spectroscopy (SIMS) and cross-sectional transmission electron microscopy (XTEM). The sheet resistance values of 250~350 ohm/sq. at a junction depth of 24 nm (at B concentration of 1.0 x $10^{18}$ $cm^{-3}$) was achieved. No significant dopant diffusion was observed after the Xe arc flash lamp annealing.**

## I. INTRODUCTION

Conventional batch furnaces have long been used for ion implant annealing in the semiconductor industry. The single wafer processing method became popular in the last decade for this application. Today, more ion implant anneal is done by rapid thermal annealing (RTA) in single wafer architectures than in batch furnaces. This is especially true for shallow junction implant annealing, RTA is believed to be a better method. A very short annealing time at higher temperature, with a very fast ramp up/down rate ("spike anneal") has been introduced as an effective shallow junction implant anneal method to electrically activate implant species with the least amount of diffusion [1 - 3]. The annealing time is now typically shorter than 1s.

For ultra-shallow junction (USJ) formation, an excimer laser-based annealing and non-filament based flash annealing techniques using arc lamps are being actively investigated [4 - 8]. The response time for the excimer laser and arc lamp is in the range of ns and ms, respectively. To eliminate the diffusion of implanted species during annealing, solid phase epitaxy (SPE) of implanted wafers at lower temperatures (600~700$^{o}$C) using RTA was also actively investigated by several research groups [9]. The temperature-time characteristics of different thermal processing techniques is summarized in Fig. 1.

In advanced Si devices, all the active device regions are located at the top surface (usually <1.0 µm from the surface) on 600~800µm thick Si wafers. Selective surface heat treatment without significant heating of the bulk Si wafer is ideal from the viewpoint of minimizing dopant diffusion to prevent defect generation during thermal processing by fast heating/cooling with minimum energy consumption Feasibility of laser thermal annealing (LTA) for ultra shallow junction implant anneal using a short wavelength (308nm), pulsed XeCl laser [4]. Two modes (surface melting and sub-melt modes) of LTA operation have been reported [10]. The surface melting mode LTA annealing gives high electrical activation efficiency, but it poses process integration problems. The sub-melt mode of LTA annealing reduces the complication of process integration in the melting mode LTA annealing and gives reasonable electrical activation of implanted species. The annealing area of both LTA modes is limited by the size of the laser beam. They require significant number of pulses, as well as scanning, using a stepper to activate the full wafer surface. In an effort of establishing practical USJ implant annealing methods, flash lamp annealing using various types of arc lamps (Ar and Xe filled arc lamps) have been actively investigated in recent years. Unlike LTA, the whole wafer surface can be annealed by a single flash in the millisecond range. Initial test results from various research groups, including the authors' group, appear very promising.

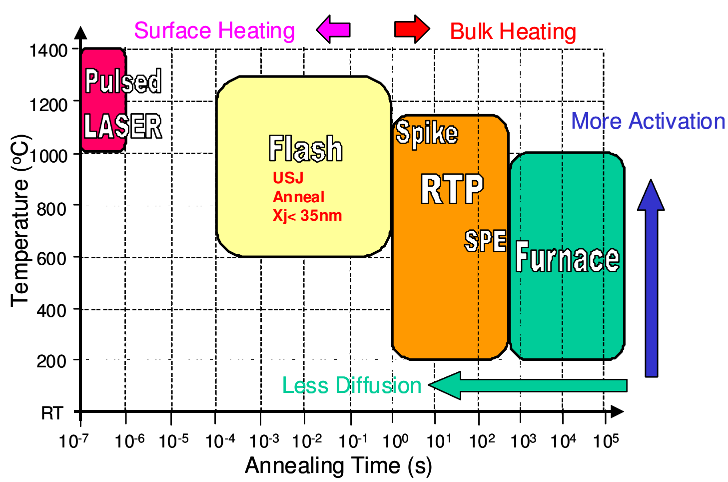


Fig. 1. Temperature-time chart of various thermal processing applications used in the semiconductor industry.

In this study, 11B+ (1keV, $1x10^{15}$ ions/cm$^2$) and $^{49}BF_2^+$ (3keV, $1x10^{15}$ ions/cm$^2$) implanted Si wafers with various implant energies and doses were annealed using a short wavelength xenon (Xe) arc lamp flash light source. The duration of the flash illumination is controlled between 1 ms and 20 ms. Annealing characteristics of ultra-shallow $^{11}B^+$ and $^{49}BF_2^+$ implanted Si wafers were also investigated in terms of electrical activation, dopant redistribution and change of junction depth ($x_j$) after annealing.

## II. Experimental

Because of the small size of the boron (B) atom, it diffuses faster in Si compared to other n-type dopants such as phosphorus (P) and arsenic (As) atoms. Both ultra-shallow ion implantation without channeling and subsequent boron implant anneal without diffusion are required for successful USJ formation. A very short annealing time, in the millisecond range, is necessary to meet the junction depth and junction abruptness requirements of USJ for the 65 nm technology node and beyond. To form an effective USJ annealing strategy for maximum electrical activation with the least amount of dopant diffusion, it is necessary to understand the fundamentals of damage recovery, solid solubility of dopants, electrical activation and dopant diffusion during implant annealing thermal cycles.

A xenon (Xe) arc lamp was used as a flash light source. The duration of flash light was controlled between 1ms and 20 ms. The flash discharge energy pulse was also controlled in the range of 0.05 MJ ~ 0.5 MJ. Samples were pre-heated up to 800°C using a hot plate in this system architecture. The emission spectrum of the flash lamp shows a maximum intensity at a wavelength about 0.3 µm and 0.4 µm (4.13 eV ~ 3.10 eV) depending on the discharge power. Tungsten halogen lamps, used for conventional RTA systems, show their maximum light intensities at about 1.1 µm ~1.4 µm (1.13 eV ~ 0.88 eV) when the filament temperature reaches about 3000°C. Since the flash lamp radiates photons of substantially shorter wavelength compared to both tungsten halogen lamps and the absorption edge (0.96 µm or 1.1 eV) of Si, it is more effective in heating the surface of Si wafer in a very short time. Figure 2 shows the light absorption spectrum of Si and the optical emission spectra for both Xe arc lamp and tungsten halogen lamps under different power conditions.

The combination of high photon energy irradiation and short flash time (<100 ms) makes possible selective ultra-fast temperature ramp of the surface without substantial heating of the bulk Si Then, a very fast temperature ramp- down of the surface layer can be achieved by conduction heat transfer from the surface to the lower temperature bulk Si. Schematic illustrations of the time-resolved surface and bulk temperature after Xe arc lamp flash are summarized in Fig. 3.

Annealing characteristics of ultra-shallow $^{11}B^+$ and $^{49}BF_2^+$ implanted Si wafers were also investigated in terms of electrical activation and dopant redistribution after annealing. Sheet resistance of implanted wafers was measured using a four point probe after annealing under various flash annealing conditions. Change in depth profiles of implant species was investigated using the secondary ion mass spectroscopy (SIMS).

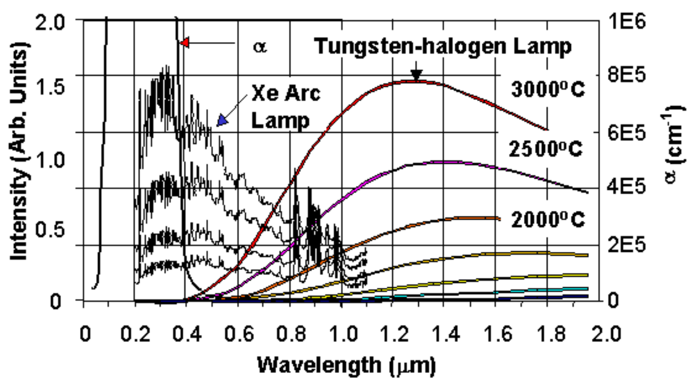


Fig. 2. Light absorption spectrum of Si and optical emission spectra from Xe-arc lamp and tungsten-halogen lamp under different power conditions.

## III. Results and Discussion

To investigate the electrical activation of implanted wafers under thermal equilibrium by ultraviolet (UV) continuous illumination, $^{11}B^+$ (1keV, $1.0x10^{15}$ cm$^{-2}$) implanted wafers were annealed for 0~20 ms using a Xe arc lamp operated at 10 kW. The junction depth $x_j$ has been traditionally defined as the depth at dopant concentration between 1.0 x $10^{18}$ cm$^{-3}$ and 5.0 x $10^{18}$ cm$^{-3}$. The as implanted junction depth $x_j$ was 37.5 nm (at 1.0 x $10^{18}$ cm$^{-3}$). As annealing time increases, sheet resistance of implanted wafers decreases due to electrical activation and the junction depth $x_j$ of annealed wafers becomes deeper because of dopant diffusion. The sheet resistance of implanted wafers annealed at sufficiently high temperature is inversely proportional to the junction depth. When the annealing time is fixed, the sheet resistance initially decreases as annealing temperature increases due to electrical activation and then decreases because of the average B concentration being reduced by diffusion. The electrical activation and dopant diffusion are competing and are both affected during annealing.

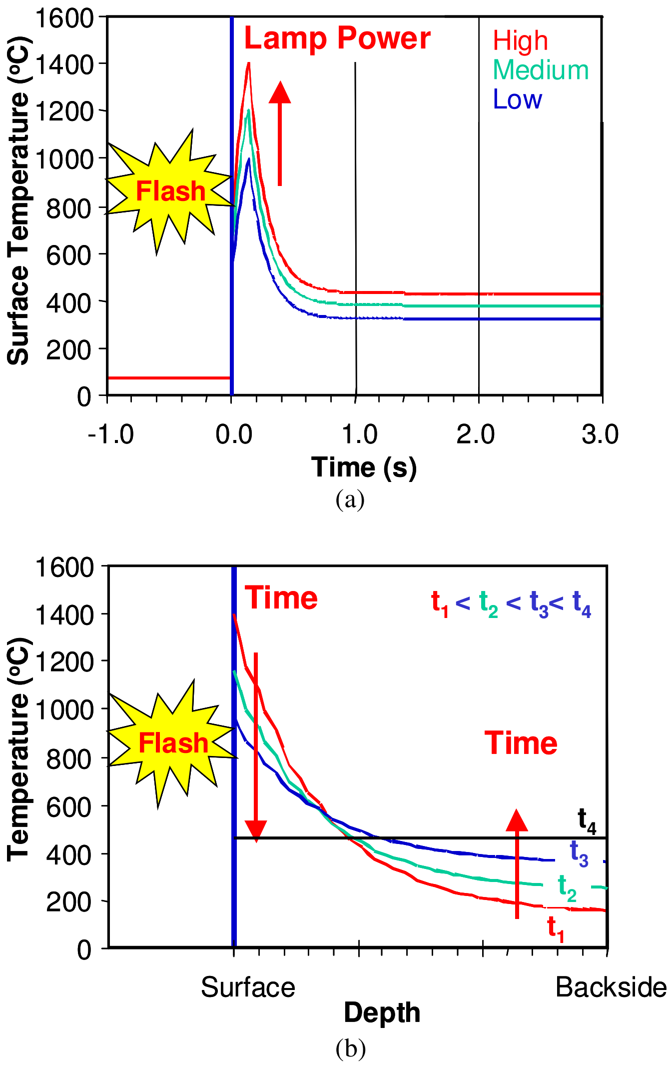


Fig. 3. Temperature profile following flash exposure: (a) Surface temperature vs. time for 3 exposures with different power, (b) Temperature vs. depth at 4 different times after flash.

The electrical activation of implanted wafers under hotplate assisted heating conditions was investigated (Fig. 4). The hot plate temperature and annealing time were fixed at 800°C and 25 s, respectively. The hot plate annealed wafer showed sheet resistance of 22.9 kΩ/sq. and the junction depth of 47.5 nm. The as implanted junction depth without Ge pre-amorphization was 37.5 nm. The hot plate anneal at 800°C for 25 s moved the junction depth by 10 nm (from 37.5 nm to 47.5 nm) without sufficient electrical activation. When a strong ultraviolet (UV) pulse (flash) from a Xe arc lamp was applied at the end of hot plate anneal, the sheet resistance was decreased to 1.7 kΩ/sq. without measurable dopant diffusion. The flash pulse power and width were 5 kJ and 10 ms respectively. Strong UV radiation for up to 1 s after hot plate anneal also decreased sheet resistance significantly without increasing the junction depth. However, additional UV irradiation for 2 s reduced the sheet resistance down to 402.2 Ω/sq. at the expense of junction movement to 60 nm. It was theorized that a combination of very strong UV flash (substantially shorter than 1 s) with preheating the wafer to slightly below the temperature for the onset of dopant diffusion (<700°C) would give ideal USJ implant annealing results (i.e. effective electrical activation without significant dopant diffusion).

SIMS depth profiles and sheet resistance values of $^{11}B^+$ (1keV, 2.0 x $10^{15}$ $cm^{-2}$ with Ge pre-amorphization) implanted wafers before and after flash annealing at different preheating temperatures are shown in Fig. 5. The as implanted junction depth $x_j$ at B concentration of 1.0 x $10^{18}$ $cm^{-3}$ was 26.0 nm. By Ge pre-amorphization, ion channeling during ion implantation was suppressed significantly (11.5 nm) from 37.5 nm to 26.0 nm. As a result, the as implanted junction depth was significantly reduced compared to the $^{11}B^+$ (1 keV, 1.0 x $10^{15}$ $cm^{-2}$) implanted wafers without Ge pre-amorphization. The flash power and width were fixed at about 25 kJ and 5 ms. Actual flash power density is not measured in this experiment. As the preheating temperature is increased, sheet resistance decreased consistently, under the same flash annealing conditions. No B diffusion was observed on flash annealed wafers at room temperature and 400°C. The wafers flashed at 700°C and 800°C showed lower sheet resistance values due to efficient electrical activation, but significant B diffusion was also observed for very short flash times (a few ms). The junction depth $x_j$ for wafers flashed at 700°C and 800°C were 34.0 nm and 56.0 nm, respectively. The wafers flashed at 800°C were 1.6 times deeper in junction depth but had 2.53 times lower sheet resistance compared to the wafers flashed at 700°C. In these wafers (flashed at 700°C), a change in B SIMS depth profile corresponding to B solid solubility (1.5 x $10^{20}$ $cm^{-3}$) was observed at 13.0 nm. A higher solid solubility (2.5 x $10^{20}$ $cm^{-3}$ at 11.0 nm) of B was observed in wafers flashed at 800°C. Under the same flash condition, the preheating temperature plays an important role in electrical activation.

The sheet resistance values of $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers were plotted in Fig. 6 as a function of junction depth $x_j$ (at B concentration of 1.0 x $10^{18}$ $cm^{-3}$) after annealing under various conditions using various annealing techniques. In the case of Xe arc lamp flash anneal, performed in this study, the sheet resistance of 250~350 Ω/sq. was achieved with a junction depth of 24 nm. The flash annealed wafers show lower sheet resistance at a given junction depth due to the efficient electrical activation with less diffusion. No significant dopant diffusion was observed after the Xe arc lamp flash annealing at room temperature and low preheating temperatures.

To achieve higher electrical activation, higher B solid solubility is required. For higher B solid solubility, high annealing temperature is a requirement. However, high annealing temperature also enhances B diffusion and makes the shallow junction ion implant anneal difficult. The high power, short wavelength flash annealing is very effective in electrically activating fast diffusing dopants, such as B, without significant diffusion and is promising as an USJ implant annealing technique for 65 nm node and beyond.

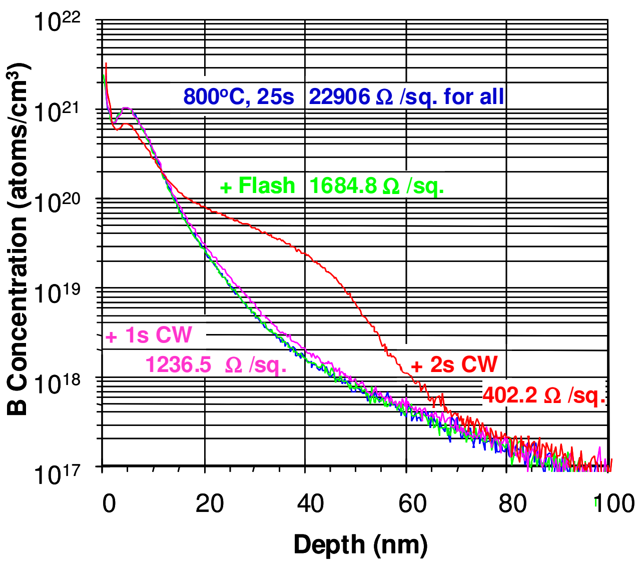


Fig. 4. SIMS depth profile and sheet resistance of $^{11}B^+$ (1keV, 2.0 x $10^{15}$ $cm^{-2}$ without pre-amorphization) implanted wafers before and after annealing.

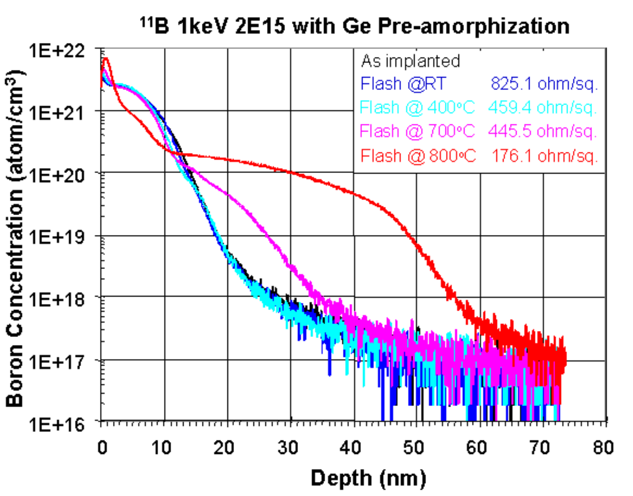


Fig. 5. SIMS depth profile and sheet resistance of $^{11}B^+$ (1keV, 2.0 x $10^{15}$ $cm^{-2}$ with Ge pre-amorphization) implanted wafers before and after flash annealing at different preheating temperatures.

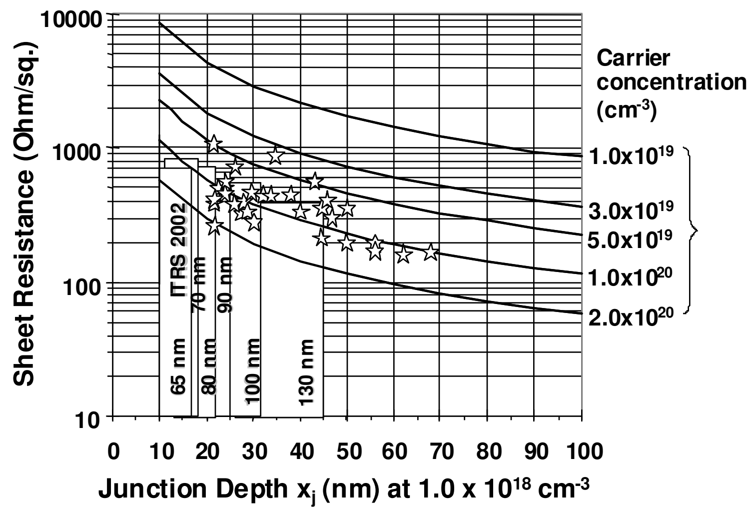


Fig. 6. Sheet resistance of $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers as a function of junction depth $x_j$ (at 1.0 x $10^{18}$ $cm^{-3}$) after annealing.

Solid phase epitaxy (SPE) (or solid phase regrowth) and changes in crystal defect density under different annealing conditions were investigated using XTEM. Both Ge pre-amorphized $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers showed very similar behavior. SPE was observed for a pre-heating temperature of 500°C. SPE is easily recognized by visual examination due to the reflectance change. The higher the SPE temperature, the lower the defect density in the junction boundary. However, even at 800°C, the SPE was not sufficient to repair all the defects. To reduce the defect density further, more high temperature annealing is required. For both Ge pre-amorphized $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers flash annealed at pre-heating temperature of 600°C, significant reduction of defects was observed despite the low pre-heating temperature. Some wafers showed no defects at all. The combination of pre-heating and subsequent flash anneal is very effective in defect reduction.

## IV. Conclusions

$^{11}B^+$ and $^{49}BF_2^+$ implanted Si wafers with various implant energies and doses were annealed using short wavelength xenon (Xe) arc lamps. The duration of flash light is controlled between 1 ms and 20 ms. Annealing characteristics of ultra-shallow $^{11}B^+$ and $^{49}BF_2^+$ implanted Si wafers were investigated in terms of electrical activation and dopant redistribution after annealing. Sheet resistance and depth profiles of implanted wafers were measured using a four point probe and SIMS. By Xe arc lamp flash annealing, sheet resistance of 250~350 ohm/sq. at a junction depth (at B concentration of 1.0 x $10^{18}$ $cm^{-3}$) of 24 nm was achieved. USJ implant anneal (higher electrical activation without dopant diffusion) was successfully demonstrated by the short wavelength Xe arc lamp flash annealing technique.

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