Ultra-Shallow Implant Anneal Using Single Wafer Rapid Thermal Furnace

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***Abstract*- A new RTA approach using a single wafer type furnace which provides wafer temperature profiles equivalent to the ones achieved from the conventional lamp-based RTA systems is introduced. The single wafer rapid thermal furnace (SRTF) allows short time annealing in a nearly isothermal furnace environment. In this paper, $^{11}B^+$ and $^{49}BF_2^+$ shallow and ultra-shallow implanted wafers (1keV~30keV) were annealed using the SRTF system to investigate electrical activation efficiency as well as B diffusion during annealing.**

I. INTRODUCTION

For ultra-shallow implant annealing applications, rapid thermal annealing (RTA) is believed to be the most effective solution to date. The pursuit of higher wafer temperature ramp rate and shorter process time had begun a few years ago. For RTA of a 200 mm diameter wafer, numerous tungsten halogen lamps are used. Initial wafer temperature ramp up rates of ~250°C/s and process time as short as 0s (named as "spike anneal") are applied in annealing ultra-shallow implanted wafers [1]. The implanted wafers are often annealed above 1000°C for 0~60s in the lamp-based RTA systems [2].

The authors have developed a new RTA approach using a single wafer type furnace which provides wafer temperature profiles equivalent to the ones achieved from the conventional lamp-based RTA systems [3]. The single wafer rapid thermal furnace (SRTF) allows short time annealing in a nearly isothermal furnace environment. In this paper, $^{11}B^+$ and $^{49}BF_2^+$ shallow and ultra-shallow implanted wafers (1keV~30keV) were annealed using the SRTF system to investigate electrical activation efficiency as well as B diffusion during annealing.

Sheet resistance and junction depth of $^{11}B^+$ and $^{49}BF_2^+$ shallow and ultra-shallow implant (1keV~30keV) with various dosage were measured after annealing under different conditions. The sheet resistance and junction depth values of implanted wafers annealed in the SRTF system was equivalent to the ones annealed using the lamp-based RTA systems. Solid solubility of B in $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers were determined as a function of wafer temperature. The implant energy, dose and annealing conditions can easily be estimated by using the solid solubility values. Fluorine segregation in $^{49}BF_2^+$ implanted wafers after annealing was also investigated in detail.

II. EXPERIMENTAL

A. *Apparatus*

A dual chamber SRTF system with a vacuum loadlock was used as the "hot wall" system (Fig.1) in this study. The process tube is made of clear quartz and has three quartz standoffs. The process tube is heated to a desired process temperature and the temperature is kept constant. A Si wafer receives thermal energy from the surrounding hot walls during annealing. For design simplicity and system reliability, the process tube uses no moving parts. The wafer is placed on the quartz standoffs (8~9 mm tall) in the middle of the quartz process tube. The separation between the wafer and the quartz walls is kept at ~10mm for both upward and downward directions. The quartz process tube is located in a SiC cavity which acts as a heat distributor to create an isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly. The temperature of the SiC cavity is monitored and controlled at a predetermined process temperature by three embedded R-type thermocouples and the three zone heater assembly. Detailed configuration, thermal characteristics and process performance of the system have been reported elsewhere [3].

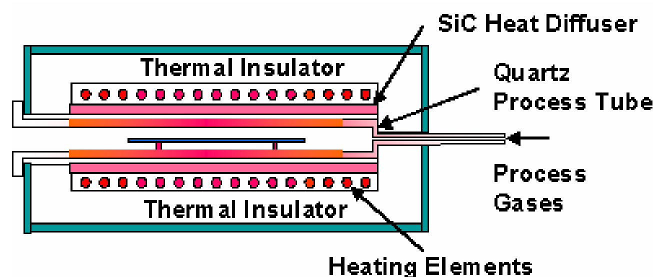


Fig. 1. Schematic illustration of wafer heating mechanisms in "hot wall" systems.

B. *Wafer Temperature Profile*

The wafer temperature profile is monitored using a thermocouple-embedded instrumentation wafer (Fig. 2). The wafer temperature was measured under 1 atm air environment using a very fine, bare R-type (Pt - 13% Rh/Pt) thermocouple bonded on the wafer. Wafer heating begins as soon as it is placed into the preheated process chamber. The wafer temperature increases rapidly and approaches the process chamber temperature in less than 20 s. The initial ramp-up rate ranges from 70°C/s to 150°C/s in the process chamber temperature range of 1000°C~1100°C. The wafer is quickly removed after the predetermined processing time at almost the process temperature. An exponential ramp-down is observed during natural cooling. Wafer cooling is normally carried out in a cooling station. The wafer temperature reaches 60°C in less than 60 s from wafer retrieval at 1100°C when cooling is carried out in the cooling station. The idle process environment temperature and wafer temperature

during the process can also be monitored using the embedded R-type thermocouple in one of the quartz standoffs.

In a SRTF system, temperature overshoot is simply not possible, and excellent temperature repeatability is realized as long as the SiC cavity temperature remains constant. The annealing time referred to in this paper is the wafer residence time (from wafer-in to wafer-out) in a heated process chamber.

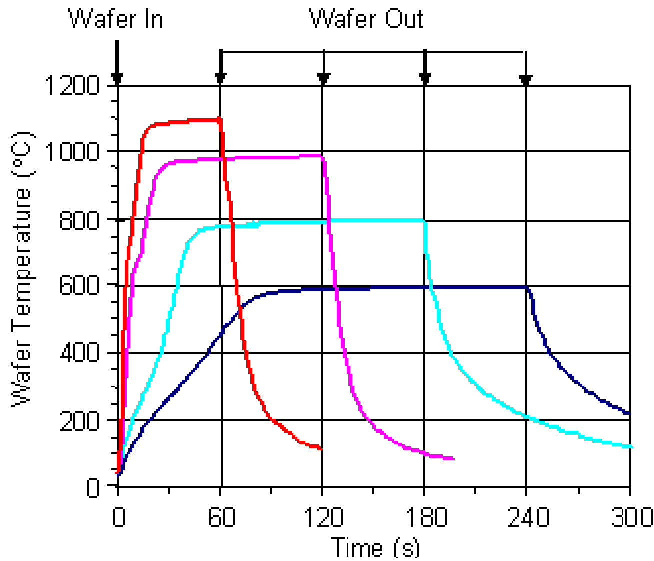


Fig. 2. Typical wafer temperature profile in SRTF system at different annealing temperatures.

C. *Specimens*

Shallow and ultra-shallow $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers were prepared. Implant energy and dosage were 1keV~30keV and $5x10^{14}cm^{-2}$ ~ $3x10^{15}cm^{-2}$, respectively. Sheet resistance and junction depth of $^{11}B^+$ and $^{49}BF_2^+$ shallow and ultra-shallow implant with various dosage were measured after annealing in the SRTF system at different annealing temperature (850°C~1100°C) and times (30~180s).

III. Results and Discussion

A. *$^{11}B^+$ Implant Anneal*

Figure 3 shows B depth profiles of $^{11}B^+$ (1keV, $1x10^{15}$ cm^{-2}) implanted wafers measured by SIMS (secondary ion mass spectroscopy) before and after annealing at 900°C for 60s~180s. As seen in the figure, junction depth (xj) of the as-implanted wafer is approximately 37nm. The xj is defined at the depth of B concentration of $1x10^{18}$ atoms/cm^{-3}. As the annealing time increases from 60s to 180s the sheet resistance decreases from 729.4 ohm/sq. to 463.71 ohm/sq. However, the junction depth xj also increases from 49nm to 64 nm.

Figure 4 shows B depth profiles of $^{11}B^+$ implanted wafers before and after annealing at 850°C for 100s~180s. At 850°C, the junction depth (xj) is around 50nm regardless of annealing time. The sheet resistance was decreased from 986.62 ohm/sq. to 816.55 ohm/sq. as annealing time increased from 100s to 180s. Longer annealing at lower temperature is promising for effective electrical activation without significant dopant diffusion during annealing.

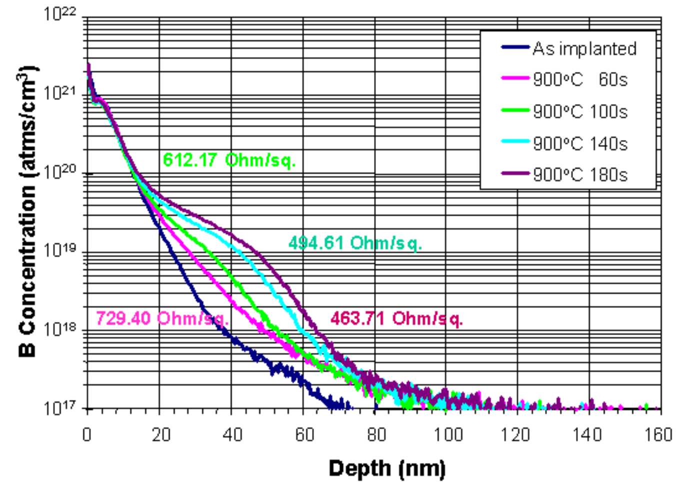


Fig. 3. Boron depth profiles before and after annealing at 900°C. ($^{11}B^+$, 1keV, $1x10^{15}$ cm^{-2})

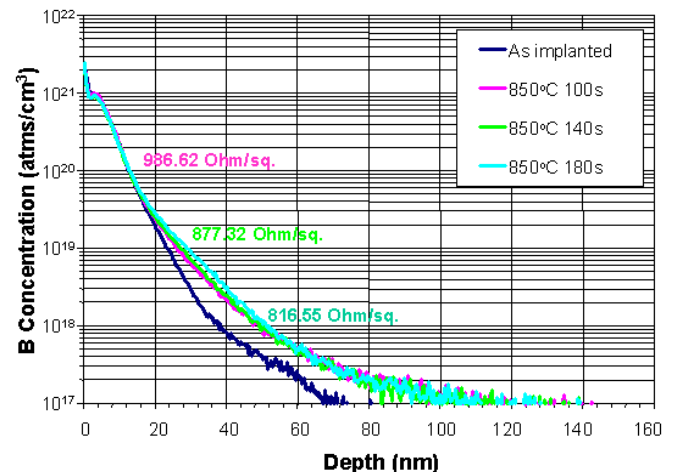


Fig. 4. Boron depth profiles before and after annealing at 850°C. ($^{11}B^+$, 1keV, $1x10^{15}$ cm^{-2})

Sheet resistance value of annealed wafers under various annealing temperature and time was plotted against junction depth xj at $1x10^{18}$ atoms/cm^3 (Fig. 5). As the annealing temperature increases, the sheet resistance decreases drastically. However, the junction depth (x)j rapidly increases due to the fast B diffusion. Excellent sheet resistance uniformity of <1%(1σ) is achieved by optimization.

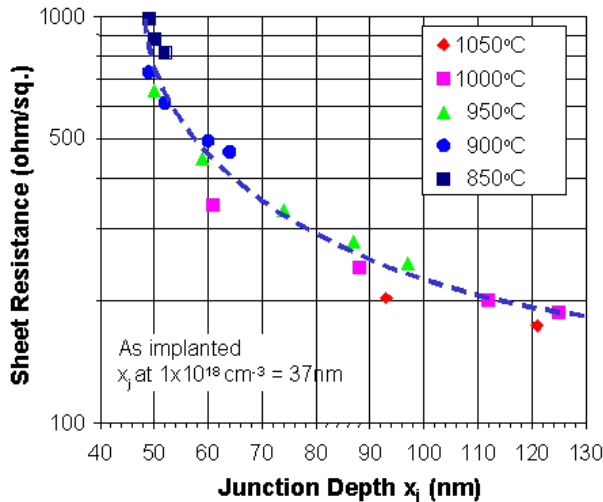
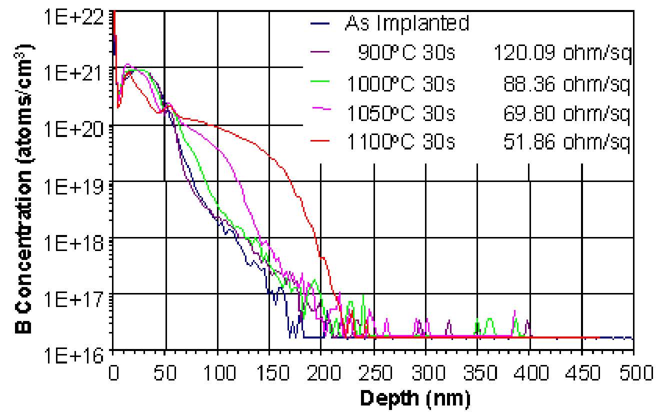


Fig. 5. Sheet resistance versus junction depth (xj) after annealing various annealing temperature and time. ($^{11}B^+$, 1keV, $1x10^{15}$ cm^{-2})

B. $^{49}BF_2^+$ Implant Anneal

Figure 6 shows B and F depth profiles of $^{49}BF_2^+$ (30keV, $3x10^{15}$ cm^{-2}) implanted wafers measured by SIMS before and after annealing at 900°C~1100°C for 30s. The sheet resistance decreased from 120.09 ohm/sq. to 51.86 ohm/sq. as annealing temperature increase from 900°C to 1100°C. The B diffused into the bulk of Si as annealing progressed. The higher the annealing temperature, the higher the B diffusion. In contrast, the as implanted F peak was split into two peaks at specific depths (20 nm and 52 nm). As annealing temperature increases, the two F peaks became weaker and sharper. The F atoms diffuse into the surface. The B and F atoms diffuse in opposite directions. Figure 7 shows the junction depth xj of as implanted and annealed wafers. The depths for F concentration of $1x10^{18}$ atoms/cm^{-3} of as implanted and annealed wafers were also plotted in the figure. The junction depth of as implanted wafer is approximately 120 nm. The xj is defined at the depth of B concentration of $1x10^{18}$ atoms/cm^{-3}. As the annealing temperature increases, the junction depth increases due to B diffusion and sheet resistance decreases due to electrical activation of implanted B and thickening of the p-type, active B doped layer. Sheet resistance uniformity of <1%(1σ) is typically achieved after process optimization.

Even after annealing at 1100°C, the majority of F atoms remained with B atoms in the implanted region. The impact of F atoms on the electrical and crystallographic properties of the implanted layer is not clearly understood. The authors have reported details of diffusion of B and F atoms in BF_2 implanted wafers during RTA using both a cold wall (lamp-based) RTA system and a hot wall (SRTF) RTA system. Similar diffusion results were observed in our previous study on BF_2 implant anneal below 1100°C regardless of the annealing system [1, 4].



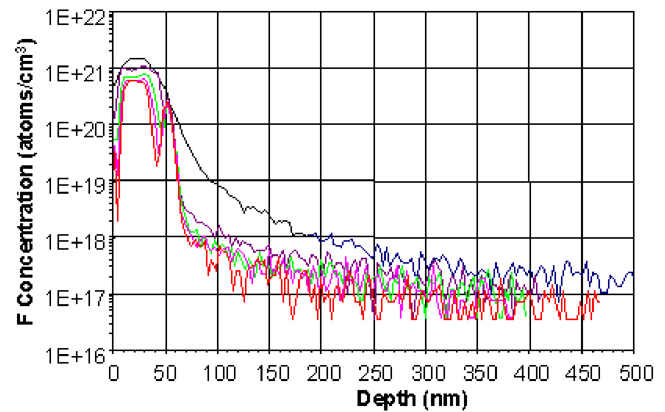


Fig. 6. Boron depth profiles before and after annealing at 900°C~1100°C for 30s. ($^{49}BF_2^+$, 30keV, $3x10^{15}$ cm^{-2})

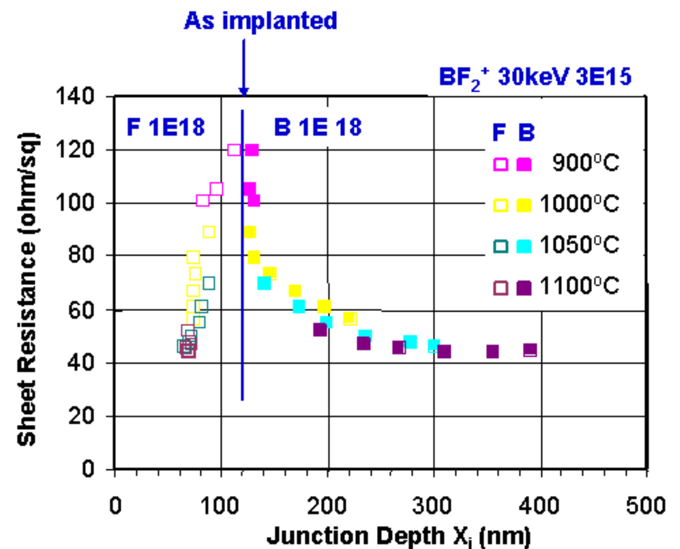


Fig. 7. Sheet resistance versus junction depth (xj) after annealing various annealing temperature (900°C~1100°C) and time (30s ~180s). ($^{49}BF_2^+$, 30keV, $3x10^{15}$ cm^{-2})

C. Discussion

RTA is believed to be the most effective solution for ultra-shallow implant annealing applications. Various types of RTA methods with high wafer temperature ramp up/down rates such as "spike anneal" [1], "excimer laser anneal" [5], "flash anneal" [6], "impulse anneal" [7] have been proposed for ultra-shallow implant annealing. All the methods utilize light absorption of Si as a wafer heating mechanism. The optical properties of Si wafers are strongly dependant on the type of dopant and dopant concentration and are further complicated by the existence of device patterns and/or foreign materials such as metal and dielectric films [8]. The varying optical properties of the object (Si wafer) being heated (illuminated) makes accurate and repeatable wafer temperature measurement and control very difficult with lamp based heating. Annealing time at maximum wafer temperature is getting shorter, approaching few hundred ms or even only a few ns. Wafer temperature is no longer steady state during annealing. This makes temperature repeatability and process uniformity on the wafer extremely difficult. Furthermore, there is a clear limitation in sheet resistance reduction without increasing junction depth (xj) significantly. Regardless of annealing methods described above, sheet resistance of shallow junctions is predetermined by the junction depth (xj) when electrical activation is sufficient. Without increasing the solubility of the solid dopant by melting the Si surface during annealing, significant sheet resistance reduction cannot easily be achieved. However, surface melting during ultra shallow junction implant anneal poses process further integration problems [5].

To achieve maximum electrical activation with minimum dopant diffusion, implant anneal must be performed at optimum (not necessarily higher) temperatures for reasonable annealing times. This process has been used in furnaces for many years. If this furnace-oriented implant anneal process is implemented in a single wafer RTP system; productivity of the system will decrease significantly. Many RTP system providers and device manufacturers focus on development of short time anneal at higher temperatures, varying wafer temperature ramp rates (up and down) for productivity enhancement. Thermal physics and process results in this study suggest the furnace-oriented implant anneal provides similar sheet resistance values obtained by the state-of-art short time ultra shallow junction anneal.

In short time annealing processes, wafers are always processed in thermal transient conditions. The transient effect is pronounced when annealing time is very short (<10 s near maximum temperature). For a given implant condition, the sheet resistance uniformity is strongly dependant upon the uniformity and stability of the thermal environment in which the wafers are processed. In a SRTF system, wafers are processed near thermal equilibrium and show superior process uniformity without sophisticated temperature control. Based on the experimental results in this study, we can conclude that equivalent sheet resistance and its uniformity were achieved in the SRTF system compared to the lamp-based RTP system. The high temperature "spike anneal" process can be replaced by a more reasonable annealing process (30~180 s annealing) using the SRTF system. In terms of process simplicity and energy efficiency, the SRTF system is superior to the lamp-based RTP systems. Energy efficiency comparisons are discussed in detail in previous papers. SRTF system also offers lot size flexibility and equivalent or better productivity compared to lamp-based RTP systems.

IV. SUMMARY

A new single wafer furnace-based RTA approach is introduced for shallow and ultra-shallow implant annealing applications. Wafer temperature profiles were measured at different annealing conditions. $^{11}B^+$ and $^{49}BF_2^+$ shallow and ultra-shallow implant (1keV~30keV) were annealed using the SRTF system to investigate electrical activation efficiency as well as B diffusion during annealing. The sheet resistance and junction depth (xj) of implanted wafers after annealing were characterized. The sheet resistance and junction depth (xj) were equivalent to the ones achieved from the conventional lamp-based RTA systems. The SRTF system is found out to be suitable for shallow and ultra-shallow implant anneal from the mass production point of view. It provides excellent process stability and repeatability at a minimum power consumption (<5kW for 1100°C annealing process).

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