Implant Anneal Using Single Wafer Rapid Thermal Furnace (SRTF) and Lamp-Based RTP System

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Abstract

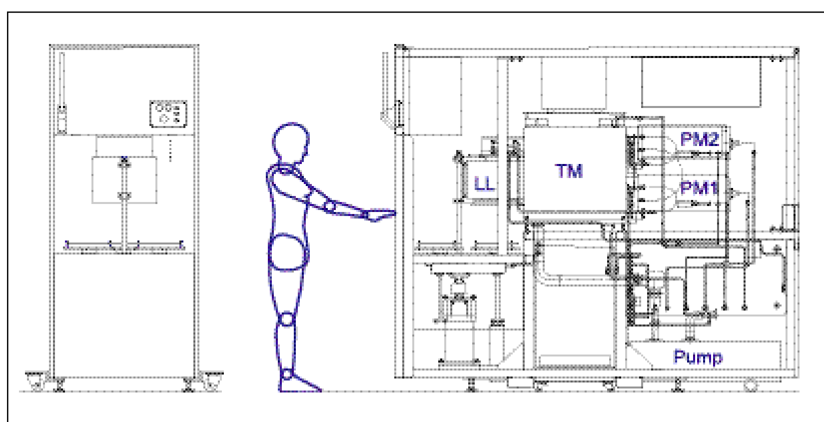
Rapid thermal annealing (RTA) of various implant species ($^{11}B^+$, $^{49}BF_2{}^+$, $^{31}P^+$ and $^{75}As^+$) in 200mm diameter Si wafers was done using a single wafer furnace (SRTF) system and a lamp-based rapid thermal processing (RTP) system under 1 atm N_2 atmosphere. Implant energy was varied between 70keV and 50keV. Average sheet resistance and its uniformity were measured after annealing under various conditions. Very efficient and uniform electrical activation across the wafer was observed in a wide range of annealing conditions. An alternative implant annealing strategy against the "spike anneal" was proposed based on experimental results.

Introduction

Lamp-based rapid thermal processing (RTP) systems have long been introduced as an alternative thermal processing equipment solution. The lamp-based RTP systems provide short cycle time, reduced thermal exposure and lot size flexibility compared to batch-type furnaces. Allowable thermal budget has decreased as device dimensions and junction depth decrease. Strong demand in thermal budget reduction and cycle time reduction made RTP become a very popular thermal processing method in recent years.

Today, many people believe that a fast wafer temperature ramp up and fast ramp down are essential for electrical activation of implanted wafers in addition to a very short annealing time. The quest for higher wafer temperature ramp up/down rates and shorter process times between RTP system manufacturers had begun several years ago. The number of tungsten-halogen lamps and power consumption during annealing process has been increased tremendously in last few years. Wafer temperature ramp up rates of ~250ºC/s and process times as short as 0s (named as "spike anneal") are often reported in literatures on state-of-the-art implant annealing, refs [1] & [2]. Implanted wafers are traditionally annealed between 800°C and 950°C for 10~30min in conventional batch furnaces, ref [3]. The same implanted wafers are annealed above 1,000°C for 0~60s in the lamp-based RTP systems. The authors believe that the high temperature short time processing requirements in the lamp-based RTP systems came from the productivity constraints. The authors asked fundamental questions regarding the effect of wafer temperature ramp up/down rates, annealing temperatures and annealing time on implant activation efficiency.

A new RTP approach using a single wafer type furnace has been proposed and it's thermal characteristics and preliminary process results have been reported, refs [4] to [7]. The single wafer rapid thermal furnace (SRTF) allows short time annealing at an equivalent wafer temperature profile achieved in lamp-based RTP systems in a nearly isothermal furnace environment at a minimal power consumption (<3.5kW per process chamber for 1,100°C process).



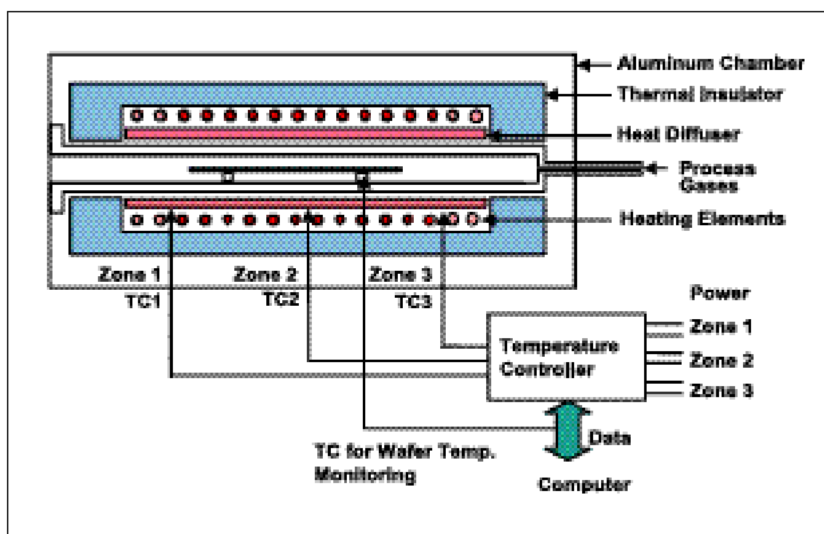


Figure 1 (top)
Schematic illustration of SRTF system

Figure 2 (above)
Schematic diagram of individual process module (furnace)

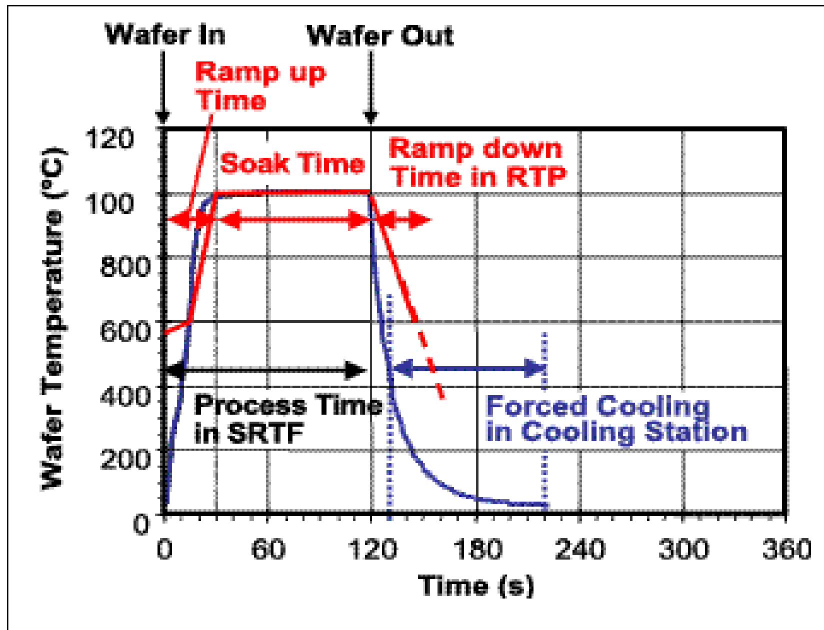


Figure 3
Schematic illustration of wafer temperature profiles during a 120s process in the SRTF system and 90s process in the lamp-based RTP system

In this paper, the authors carried out an implant annealing study using the SRTF system to investigate the effect of annealing temperature and annealing time on implant activation efficiency. For comparison, implant annealing was done using a conventional lamp-based RTP system. Production-worthy implant annealing process results of the furnace-based SRTF system were discussed in detail. An alternative implant annealing strategy against the "spike anneal" was proposed based on the process results.

EXPERIMENTAL

SRTF System

Schematic diagram of a dual chamber SRTF system with a vacuum loadlock used in this study is shown in Figure 1. Two vertically stacked process chambers (furnace), a vacuum loadlock and two cooling stations are attached to the wafer transport module. By stacking two furnaces, the footprint of the system is greatly reduced. The cross-section of the individual process modules (furnace) is illustrated in Figure 2. The process tube is made of clear quartz and has three quartz standoffs. The process tube uses no moving parts for simplicity and system reliability. The wafer is placed on the quartz standoffs (8~9mm tall) in the middle of quartz process tube. The distance between the wafer and the quartz walls is kept at ~10mm in both upward and downward directions. The quartz process tube is located in a SiC cavity which acts as heat distributor to create an isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly. The temperature of the SiC cavity is monitored and controlled at a predetermined process temperature by three embedded R-type thermocouples and a three zone heater assembly to provide an identical and nearly isothermal environment to wafers regardless of wafer types and conditions. Detailed configuration, thermal characteristics and process performance of the system has been reported elsewhere, refs [4] to [7].

Lamp-based RTP System

The lamp-based RTP system used in this study employs banks of linear tungsten halogen lamp arrays which illuminate a Si wafer from the top and bottom sides through the quartz process tube. Wafer temperatures are measured using a pyrometer viewed through the quartz tube. A multiple zone power control method is used to adjust temperature uniformity on the Si wafer. Wafer temperature ramp-up rate, soak time and ramp-down rate are programmable.

Experimental

Implant wafers were annealed using the SRTF system and lamp-based RTP system in a mass production environment after characterising thermal characteristics of the system. 200mm diameter Si wafers implanted with various species were annealed using the SRTF system and lamp-based RTP system under 1 atm N_2 atmosphere to compare resulting sheet resistance and its uniformity after annealing. The annealing temperature was varied between 900°C and 1,100°C. Figure 3 shows a typical wafer temperature profile during processing at 1,000°C. Process time (wafer residence time in furnace) for the SRTF system in the temperature range of 900°C~1,100°C can be easily estimated by simply adding 30s to the "soak time" in the lamp-based RTP system because it is approximately equal to "ramp up time" plus "soak time" in the lamp-based RTP system. Average sheet resistance measurement after implant anneal at 1000°C using the SRTF system and lamp-based RTP system indicated that the estimated process time for the SRTF system (30s addition to the "soak time" in the lamp-based RTP system) gives an equivalent average sheet resistance after annealing.

The annealing time for the SRTF system was varied between 40s and 180s. The annealing time for the lamp-based RTP system was varied between 10s and 150s. The sheet resistance of annealed wafers were measured at 49 points using a four-point probe with a 5mm edge exclusion during the sheet resistance measurement. Surface response of sheet resistance and its uniformity were used for process window determination. Dopant depth profiles were also measured before and after annealing using a secondary ion mass spectroscopy (SIMS) to investigate dopant diffusion during annealing.

RESULTS AND DISCUSSIONS

Average sheet resistance and sheet resistance uniformity plots of four different types of implanted wafers ($^{11}B^+$ 50keV $1x10^{15}$ cm^{-2}, $^{49}BF_2^+$ 70keV $1x10^{15}$ cm^{-2}, $^{31}P^+$ 70keV $1x10^{15}$ cm^{-2} and $^{75}As^+$ 70keV $1x10^{15}$ cm^{-2}) were plotted in Figure 4 (a) and (b) as a function of process (annealing) temperature. Process (annealing) time was fixed at 70s (from wafer-in to wafer-out) for the SRTF system and 30s (soak time at process temperature) for the lamp-based RTP system. All four kinds of implanted wafers were electrically well activated above 1,000°C regardless of wafer heating method (annealing system). Equivalent average sheet resistance values were achieved in wafers annealed using both systems. A higher temperature sensitivity of sheet resistance was observed in $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers compared to those in $^{31}P^+$ and $^{75}As^+$ implanted wafers. The sheet resistance uniformity in all four different types of implanted wafers ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and ^{75}As) annealed at 900°C and 1,000°C using the SRTF system was below 1.0% (1s). $^{49}BF_2^+$ and $^{75}As^+$ implanted wafers showed slight increase of sheet resistance uniformity values after annealing at 1,100°C while the average sheet resistance value remain constant.

In case of the lamp-based RTP system, all four different types of implanted wafers ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$) annealed at 1,000°C showed the sheet resistance uniformity below 1.0% (1s). At annealing temperatures of 900°C and 1,100°C, sheet resistance uniformity values of most implanted wafers exceeded

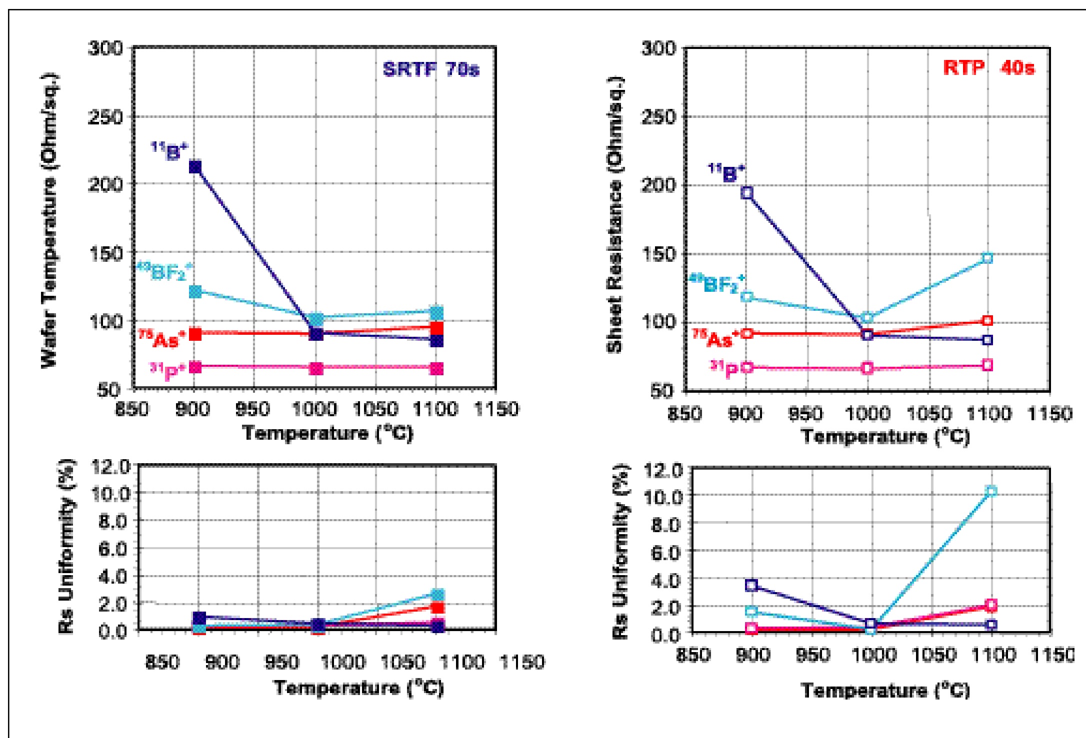


Figure 4
Average sheet resistance and its uniformity on implanted wafers after annealing in SRTF system (a) and lamp-based RTP system (b)

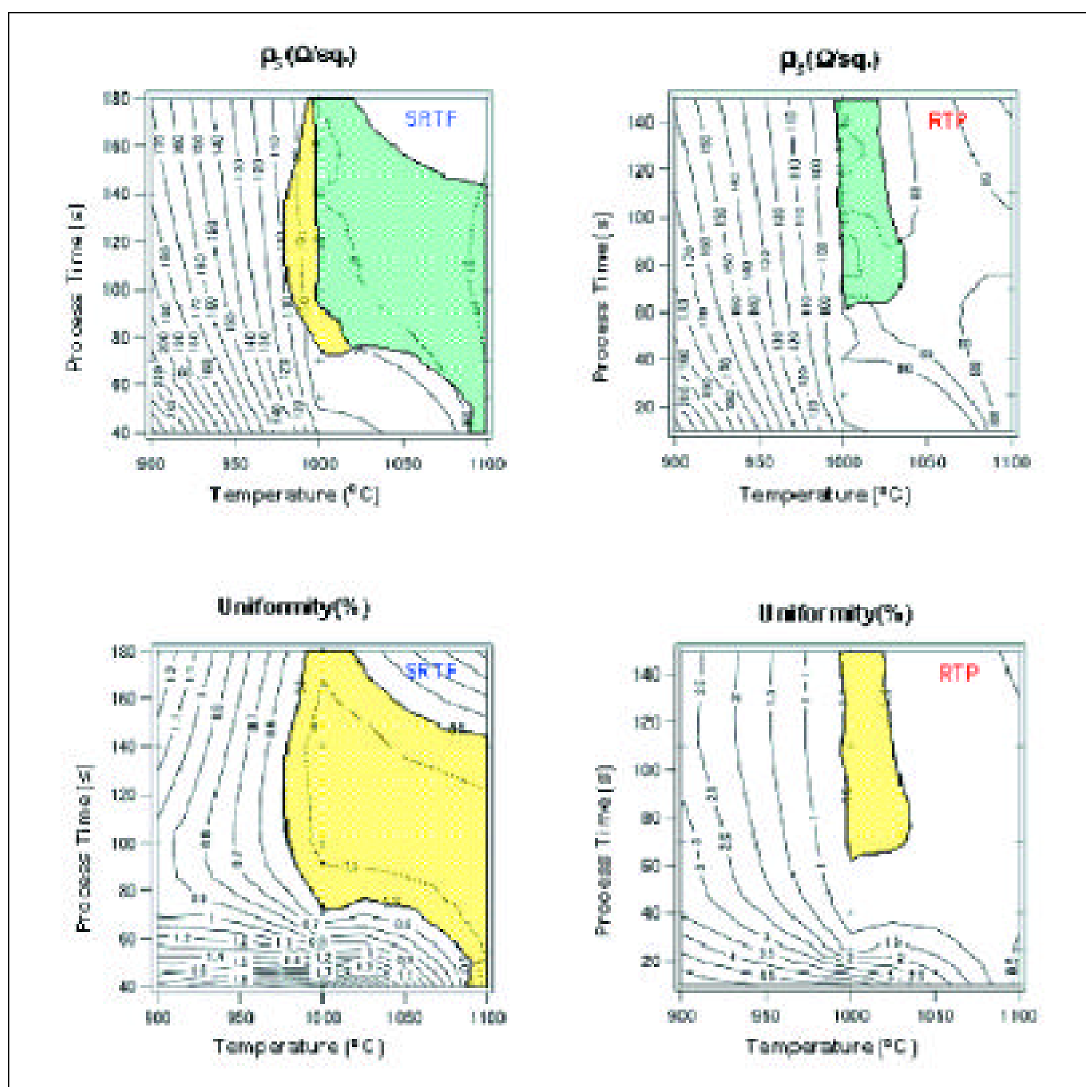


Figure 5
Surface response maps and process window of average sheet resistance and its uniformity after annealing in SRTF system and lamp-based RTP system

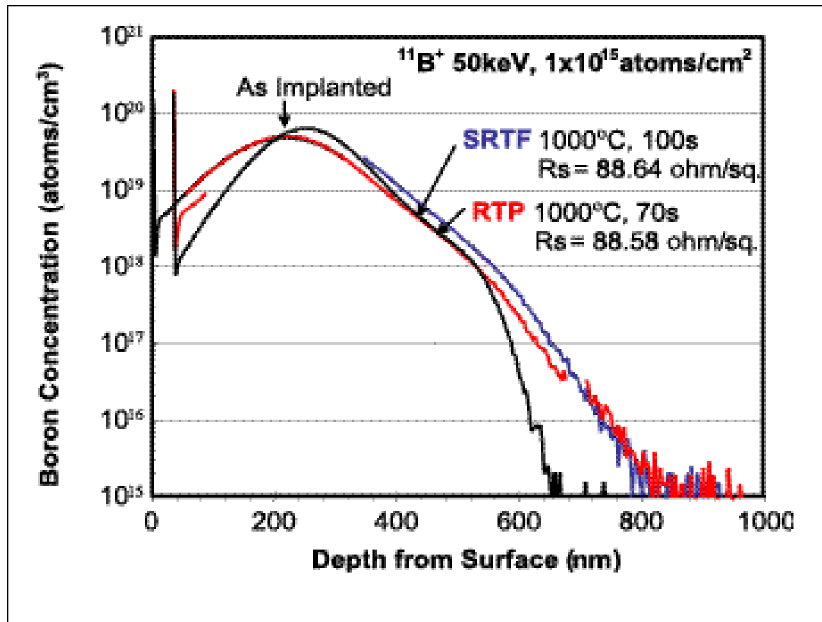


Figure 6
SIMS depth profiles of as-implanted wafer and wafers after annealing in SRTF and lamp-based RTP systems

1.0% (1W). In the case of $^{49}BF_2^+$ implanted wafers, both average sheet resistance and its uniformity values significantly increased after annealing at 1,100°C. The average sheet resistance value was increased from 102.6 ohm/sq. at 1,000°C to 146.4 ohm/sq. at 1100°C. The sheet resistance uniformity value in 1s was also significantly increased from 0.25% (at 1,000°C) to 10.22% (at 1,100°C) after annealing. Fluctuation of boron concentration in the depth direction due to boron segregation was observed in $^{49}BF_2^+$ implanted wafers annealed at 1,100°C for greater than 25s. The boron segregation is responsible for the abnormal average sheet resistance and its uniformity increase in wafers annealed at 1,100°C. The boron segregation mechanism is currently under investigation.

Surface response of average sheet resistance and sheet resistance uniformity of $^{11}B^+$ (50keV 1x10^{15} cm^{-2}) implanted wafers are shown in Figure 5 as a function of annealing temperature and time. As seen in the figures, behavior of the average sheet resistance and sheet resistance uniformity in annealed wafers is very complex. In wafers annealed using the SRTF system, sheet resistance decreases as annealing temperature and annealing time increases due to electrical activation of implanted species. As seen in the Figures 2 and 3, the sheet resistance values are very sensitive to annealing temperature in the temperature range of 900°C and 1,000°C regardless of annealing system. In terms of sheet resistance uniformity, the SRTF system provides a wide window for annealing conditions. Process windows for $^{11}B^+$ (50keV 1x10^{15} cm^{-2}) implanted wafers in the SRTF system and lamp-based RTP system were determined by using the average sheet resistance value of < 90ohm/sq. and the sheet resistance uniformity value of < 0.5%(1s) as criteria. The process windows in each system are indicated in Figure 5. The sheet resistance uniformity was the limiting factor for the process window in both the SRTF system and lamp-based RTP system. In general, longer annealing at lower temperatures gives lower average sheet resistance and better sheet resistance uniformity regardless of annealing system.

Figure 6 shows SIMS depth profiles of as implanted ($^{11}B^+$ 50keV, 1x10^{15} atoms/cm^{-2}) wafer and wafers annealed at 1,000°C in the SRTF and lamp-based RTP systems. Annealing times for the SRTF and lamp-based RTP systems were 100s (wafer-in to wafer-out) and 70s (soak time), respectively. Diffusion of boron atoms toward the surface and depth direction was observed after annealing. Both average sheet resistance and SIMS depth profiles of wafers annealed using different types of annealing systems became very close to each other.

$^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$ implanted wafers showed average sheet resistance increase with increase in annealing temperature (> 1,000°C) and time while $^{11}B^+$ implanted wafers showed decreases in average sheet resistance. The average sheet resistance increase with increase in annealing temperature and time can be explained by the thermal diffusion of implanted species in the wafer. As thermal diffusion progresses, the dopant concentration in the implanted region decreases and resulted in an increase of the average sheet resistance.

To understand the physics behind the implant anneal, we need to review how the implant anneal is done in conventional batch furnaces. It takes place in temperature range of 800°C~950°C for 10~30min, ref [3]. Very consistent average sheet resistances and sheet resistance uniformity are achieved. However, the conventional batch furnace lacks lot size flexibility and requires a longer cycle time.

Three main reactions take place in parallel during implant anneal. They are (1) recrystallisation (solid phase regrowth) of the damaged (amorphised) layer during implantation, (2) electrical activation of implant species and (3) thermal diffusion of the implanted species. Full recrystallisation of the amorphised layer and full electrical activation of implant species without thermal diffusion would be the ideal for implant anneal. It is well known that the solid-phase regrowth occurs at a temperature as low as 450°C. Solid-phase regrowth rates of (100) silicon at 600°C and 800°C are approximately 1nm/s and 500nm/s, respectively, ref [8]. Electrical activation and dopant diffusion require higher thermal energies to take place. There are two well known facts: (1) diffusivity of atoms in Si increases exponentially as annealing temperature increases and (2) the increase in diffusion length is proportional to square root of annealing time at a given temperature, ref [9]. Thus, total diffusion length is proportional to the square root of the product of diffusivity and time.

To achieve maximum electrical activation with minimum dopant diffusion, the implant annealing process must be optimised in terms of annealing temperature and annealing time. For the production-worthy repeatable process results on the average sheet resistance and sheet resistance uniformity, a reasonable amount of annealing time at an optimum temperature is desired rather than a 'spike anneal' at maximum temperature.

We can conclude that the SRTF system offers equivalent or better implant annealing process results and higher productivity compared to the lamp-based RTP system. The SRTF system also offers a single wafer signature, lot size flexibility and high energy efficiency, refs [4] to [7]. Many RTP applications including implant anneal can be performed using the SRTF system.

SUMMARY

Comparative RTA study of various implant species ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$) in 200mm diameter Si wafers was done using a resistively heated, SWF system and lamp-based conventional RTP system under 1 atm N_2 atmosphere. Average sheet resistance and sheet resistance uniformity were measured after annealing under various conditions. Production worthy process windows for SRTF and lamp-based conventional RTP systems are also

compared. Lower average sheet resistance and superior sheet resistance uniformity were achieved in wide process conditions using SRTF system. The effect of annealing on dopant redistribution was investigated using SIMS. The validity of the 'spike anneal' was discussed based on electrical activation and dopant diffusion mechanisms in implanted Si wafers.

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