Thick copper inter connection annealing process development using a mini-batch stacked annealing oven

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ABSTRACT

A Cu annealing process was characterised using an ambient controlled, stacked hot plate-based annealing system in the temperature range of 100ºC~450ºC. The effect of annealing conditions on Cu interconnects of various thickness was investigated as a function of annealing temperature, time. Sheet resistance of the Cu films was reduced by 21~23% after annealing. The grain size increased significantly during annealing and was primarily determined by annealing temperature. No correlation was observed between sheet resistance reduction and grain size growth. The electrical and crystallographic characteristics of Cu films annealed using the hot plate-based annealing system were compared with self-annealed Cu films. A production worthy Cu annealing process with a wide and repeatable process window has been developed using the hot plate-based stacked annealing oven.

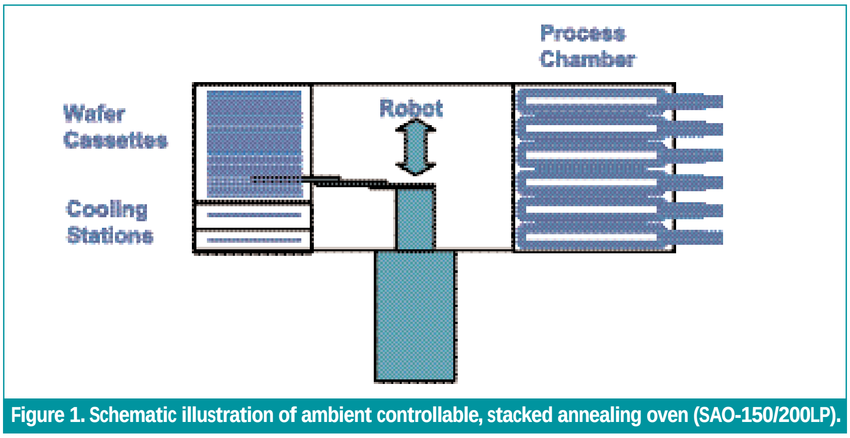


Figure 1. Schematic illustration of ambient controllable, stacked annealing oven (SAO-150/200LP).

INTRODUCTION

Copper (Cu) was introduced several years ago to replace aluminium (Al) interconnections in ultra-large scale integration (ULSI) logic devices in order to produce small dimension, higher speed devices. [1] The electrical resistivity of Cu is 1.7x10^{-6} Ω.cm versus 3x10^{-6} Ω.cm for Al. [2] Consequently, it is possible to reduce the width of interconnections without affecting device performance or to operate at higher frequencies by reducing the resistive value of the RC equivalent circuit of on-chip interconnects (combined with a decrease of the capacitance by using low k dielectric layers). The higher thermal conductivity of Cu (4.01 W cm/K at 300K) over Al (2.37W cm/K at 300K) is an added benefit. [2]

The high electrical and thermal conductivity of Cu are very attractive for applications for ULSI logic devices as well as for smart power devices. The high electrical conductivity of Cu allows high current flow per unit area with less joule heat generation. High thermal conductivity also helps efficiently dissipate the heat generated by current flow during device operation. Although the properties of Cu as an interconnect and heat dissipation material are very attractive for IC manufacturing, integration of Cu into ICs and understanding its properties, including the effect of annealing, are still a technical challenge.

Electrochemically deposited (ECD) Cu films are unstable crystallographically and electrically (grain growth and sheet resistance undergo changes) [3] so, for proper use, stabilization is required. Cu is also easy to oxidize in air even at relatively low temperatures (~200°C) and forms CuO layer with higher resistivity. [4] Due to these unique characteristics, process integration of Cu (including diffusion barrier formation, Cu ECD, Cu annealing and passivation) has not been easy [5-6].

The aim of this work was the study of the effect of Cu annealing on its electrical and crystallographic properties compared with the self-annealed ones. In this study, a thick copper layer, introduced on Smart Power circuits to reduce R_{ON} of LDMOS transistors, has been grown through a thick photoresist mask by ECD. In particular, Cu annealing was performed using a mini-batch, stacked hot plate-based annealing system under various conditions of annealing time and temperature. Some production worthy Cu annealing processes were then developed.

EXPERIMENTS

Experimental Apparatus

A hot plate-based, stacked annealing oven (WaferMasters SAO-150/200LP) for 150mm or 200mm wafers was used in this study. The SAO-150/200LP annealing system was designed for low temperature annealing applications in the temperature range of 100~550°C and is capable of processing five wafers simultaneously under controlled process gas environments. It was designed to provide single wafer signature, lot size flexibility and reasonable productivity with minimum facility requirements. A schematic illustration of the SAO-150/200LP system is shown in Figure 1. The system consists of a wafer cassette, wafer handling robot, process chamber and cooling stations. All the process related components are located within a leak tight enclosure. When process gas ambient control is needed, the system is evacuated by using a dry vacuum pump and backfilled with the desired gas such as forming gas (N_2 + H_2 mixture) or pure N_2. Residual O_2 concentration below 5 ppm is easily achieved by simple pump and purge cycles.

Figure 2 shows a side view of the stacked hot plates with five Si wafers. The design allows gradual heating of wafers for low temperature annealing and baking applications without sacrificing productivity. The individual hot plates are made of aluminium and have an embedded heater for temperature control. Aluminium was chosen as the hot plate material for temperatures up to 550ºC because of its thermal stability, high thermal conductivity and ease of machining. The hot plate is slightly larger in diameter and significantly thicker (30mm) than the Si wafer. The individual hot plates have three stand-offs to maintain accurately the distance between the wafer and the hot plate surfaces.

The stand-offs are equally spaced on the perimeter at approximately 70% of wafer diameter. The gap between the hot plates is 20mm. The wafers are located at the middle of the top and bottom hot plates (10 mm above the bottom hot plate and 10mm below the top hot plate). The wafers are heated by natural convection and conduction through ambient gas as well as by radiation. Hot plate temperature and process gas pressures are controlled and accurately determine the wafer temperature profile. For lower thermal conductivity gases such as N_2, O_2, Ar or air, wafer temperature rises and approaches the hot plate temperature [7]. For gases with higher thermal conductivity such as H_2, He and forming gas containing H_2 gas, wafer temperature rises more rapidly and approaches the hot plate temperature. Wafer temperature profiles under different hot plate temperature and process gas conditions are plotted in Figure 3.

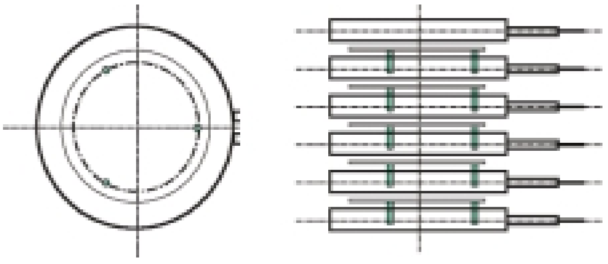


Figure 2. Top and side view of stacked hot plates.

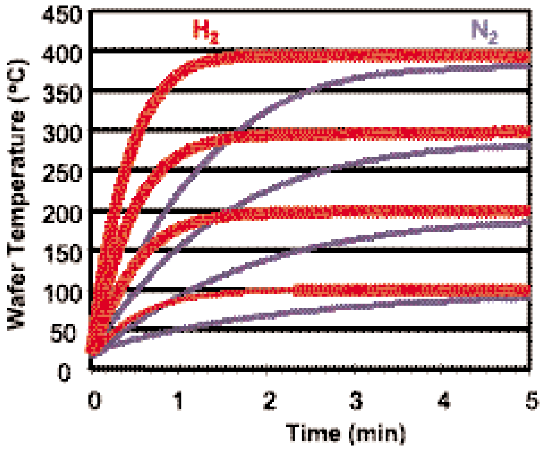


Figure 3. Wafer temperature profile at different hot-plate temperatures under 1 atm H_2 and N_2 ambient.

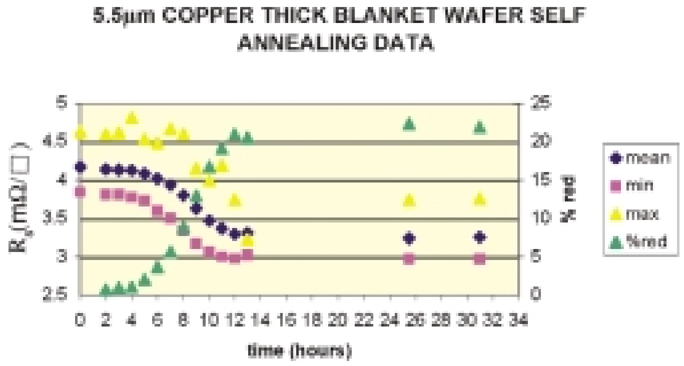


Figure 4. R_S variation versus time; mean, maximum and minimum value; % R_S reduction.

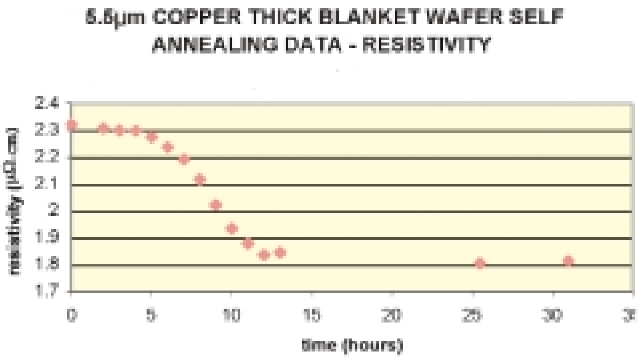


Figure 5. Resistivity reduction versus time; mean value calculated from mean R_S and mean data values for thickness.

SAMPLE PREPARATIONS

After sputtering a barrier layer (60nm TiN) and a Cu seed layer (100nm), Cu films, 3µm and 5.5µm thick, were electrochemically deposited (ECD, Semitool Equinox tool) on 6 inch blanket and patterned wafers. Blanket wafers were prepared by ECD with no further treatment done on their surface, while patterned wafers were grown by ECD through a thick photoresist mask that was then removed before the subsequent self-annealing or SAO annealing treatment. The annealing temperature and time were varied, respectively, from 100°C to 450°C and between 2 and 15 min. To avoid Cu oxidation during annealing, an O_2-free process environment was chosen. The chamber was evacuated and filled with forming gas (N_2 95% + H_2 5%) before annealing. Sheet resistance, uniformity, grain size and crystallographic orientation were investigated as a function of annealing temperature and time.

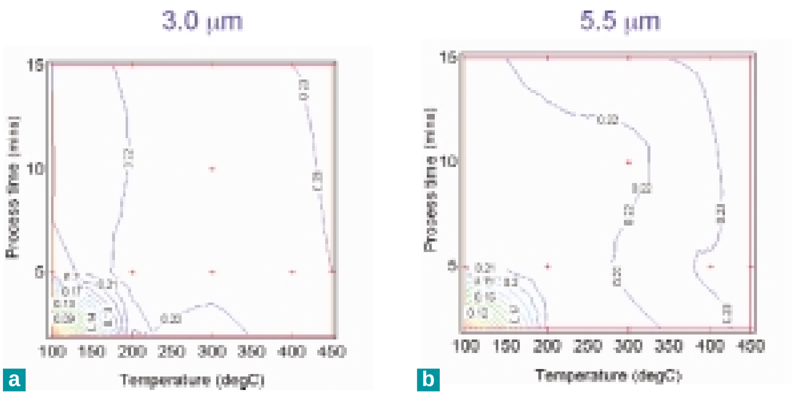


Figure 6. Surface response of the sheet resistance reduction ratio of Cu films as a function of annealing temperature and time.

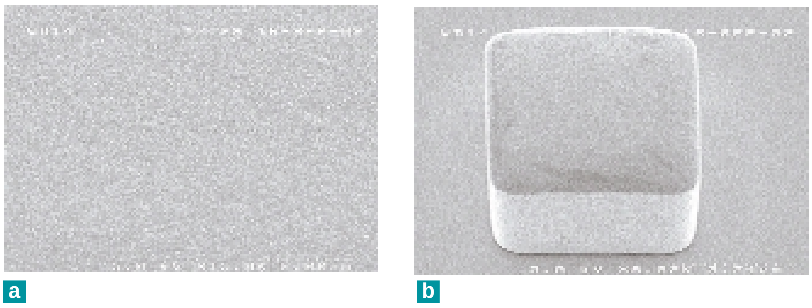


Figure 7. SEM images of a 5.5 µm thick copper self annealed wafer.

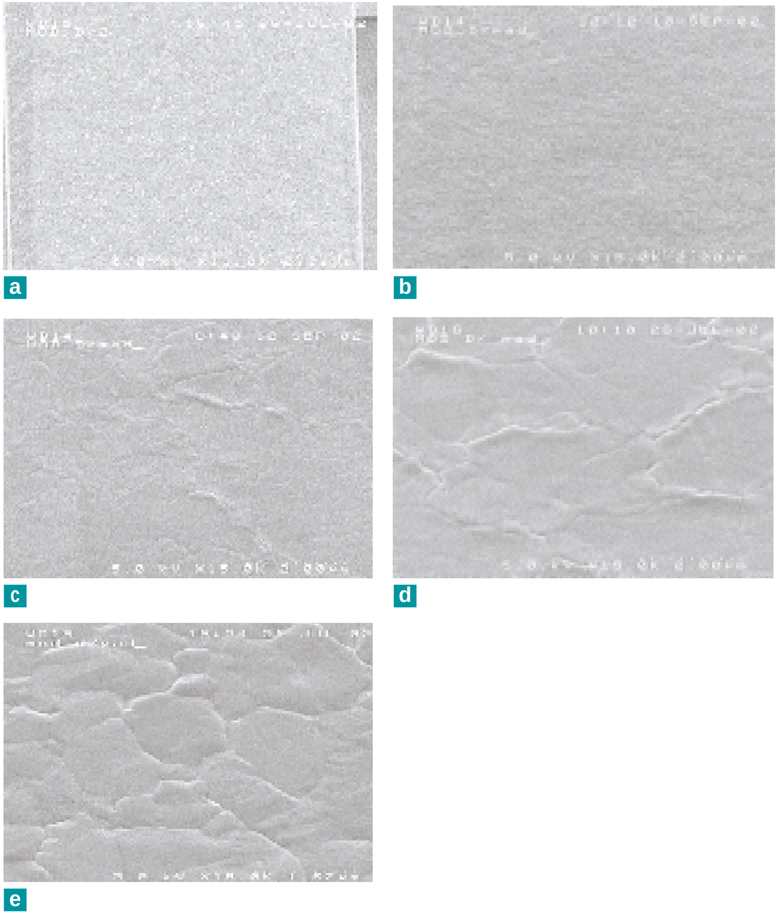


Figure 8. SEM images of 5.5µm thick copper wafers annealed for 15 minutes at: a. 100ºC; b. 200ºC; c. 300ºC; d. 400ºC; e. 450ºC.

RESULTS & DISCUSSIONS

Sheet resistance measurement

Self-Annealing. Sheet resistance (R_S) of a 5.5 µm Cu film on a blanket wafer was measured just after plating (i.e. «as grown») and its trend versus time was then recorded until 31 hours after plating. A Four Point Probe Prometrix was used to measure R_S on a 49 points map and the same 49 points map was used to measure Cu thickness. The instrument used is an XRF Veeco 5300. The R_S trend versus time is shown in Figure 4 while the resistivity reduction versus time is shown in Figure 5. The resistivity value varies from 2.32 µΩ.cm immediately after growth, to 1.80 µΩ.cm after self-annealing process completion, reaching 21~23% reduction. The resistivity value doesn't change from 12 to 31 hours of self-annealing time, thus the self-annealing process for a 5.5 µm Cu film can be considered completed after about 12 hours from growth.

SAO-Annealing. Sheet resistance measurements have been carried out on Cu blanket wafers after annealing. All the Cu blanket wafers were measured before and after annealing in order to get R_S reduction data. As a reference, all SAO treatments were always performed one hour after plating since the self-annealing has not yet started .

Figure 6 (a) and (b) shows sheet resistance reduction of 3.0 µm and 5.5 µm thick Cu films on blanket wafers as a function of annealing temperature and time. As temperature and time increase, the sheet resistance was reduced drastically regardless of Cu film thickness. Both surface responses, in Figures 6, suggest that when the annealing temperature is higher than 200°C or annealing time is longer than 5 min, the sheet resistance is reduced by 20% or more. Once this value is achieved, no additional reduction is observed even after further annealing. Sheet resistance uniformity for 3.0 µm and 5.5 µm thick Cu films on blanket wafers is not affected by any thermal annealing.

To summarise there is no significant difference in sheet resistance between self-annealed and thermally annealed Cu thick wafers if the temperature exceeds a base value (typically more than 200ºC) and the annealing time is longer than about 5 minutes.

GRAIN GROWTH OBSERVATION

Surface morphology of a 3.0µm and

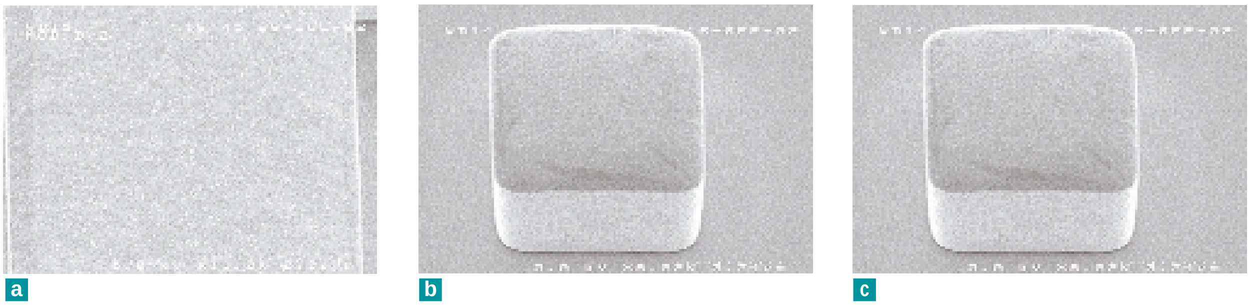


Figure 9. SEM images of 5.5 µm thick copper wafers annealed at 300ºC for: a. 2 min; b. 5 min; c. 10 min.

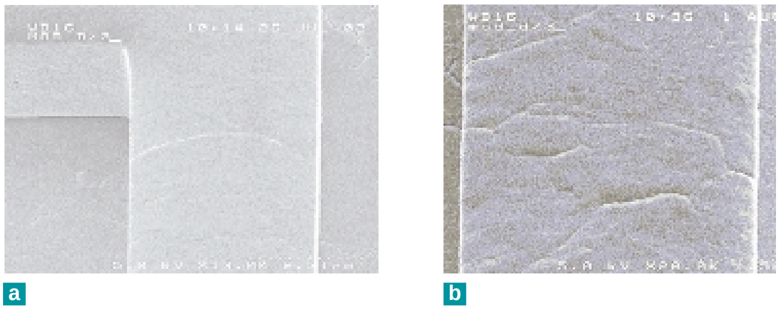


Figure 10. SEM images of: a. 5.5µm thick copper wafer annealed at 400ºC for 15 minutes; b. 5.5µm thick copper wafer annealed at 450ºC for 15 minutes. The strips are 5µm wide in both cases.

5.5µm Cu film on a patterned wafer under different conditions of annealing was observed by scanning electron microscopy (SEM – Hitachi 4620). Since no significant difference was encountered between the two wafer types, the discussion will be based on 5.5µm Cu thick wafers only. The self-annealed sample doesn't show any evidence of a well-defined grain structure as reported in Figure 7.

The effects of temperature and annealing time were investigated separately. Figure 8 (a – e) shows five different Cu surfaces of wafers annealed with the same annealing time (15 minutes) at different annealing temperatures.

For annealing temperatures of 100°C and 200°C no significant grain size appears while as annealing temperature increases, grain size grows significantly. In fact at 300°C, a defined grain structure begins to appear. A very distinct grain structure develops at 400°C and the grain dimension is around 5 µm (see Figure 10a); at 450°C it is even larger (see Figure 10b). Since the grain growth becomes evident starting from 300°C, the effect of annealing time is investigated at this temperature and shown in Figure 9. The combination of annealing time and temperature for a well-defined grain growth formation starts from 300°C 15 minutes. All the investigated combinations of these two parameters below the above mentioned values do not contribute to the grain growth structure. On the other hand, at higher temperature significant grain growth structure appears even at much shorter annealing time. This SEM analysis shows that thermally annealed wafers are very different in terms of grain size depending on annealing time and temperature, despite R_S analysis results that did not show this difference.

Apparently there is no strong correlation between grain growth of Cu films and sheet resistance reduction. A further experiment was made to confirm this. A self-annealed wafer with a resistivity value of 1.8μΩ.cm was then treated at 450ºC for 15 min in forming gas (N_2 95% + H2 5%) at 1 atmosphere. This wafer, that didn't show any grain definition by SEM inspection before thermal treatment, developed a defined grain structure after the annealing keeping the same resistivity value. Furthermore in order to check the stability of annealed Cu grain structure, an additional wafer, already annealed at 300ºC for 15 minutes, was subsequently treated at 450°C for 15 minutes. No change in grain dimensions and resistivity value were encountered.

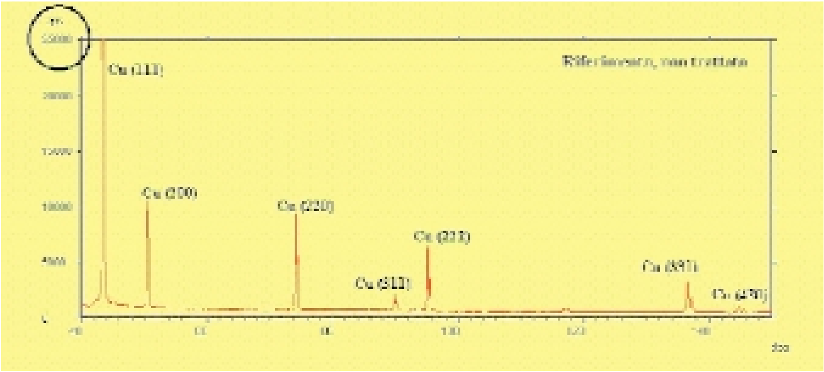
It is well known that ECD Cu films subjected to a 'self-annealing' at room temperature undergo a reduction of sheet resistance from the 'as grown' level. [3] However, self-annealed Cu films did not show grain growth despite this change in sheet resistance. The consistent change in sheet resistance, independent of annealing temperature lead many researchers to assume the reduced-resistivity Cu film was stable. The experiments done suggest that the grain size could be considered a better parameter to be measured for determining film stability and therefore the annealing treatment plays a crucial role.

X-RAY DIFFRACTION

To investigate the preferred crystallographic orientation of Cu grains after annealing, X-ray diffraction (XRD) analysis was performed. The "Bragg-Brentano" method of analysis was used.

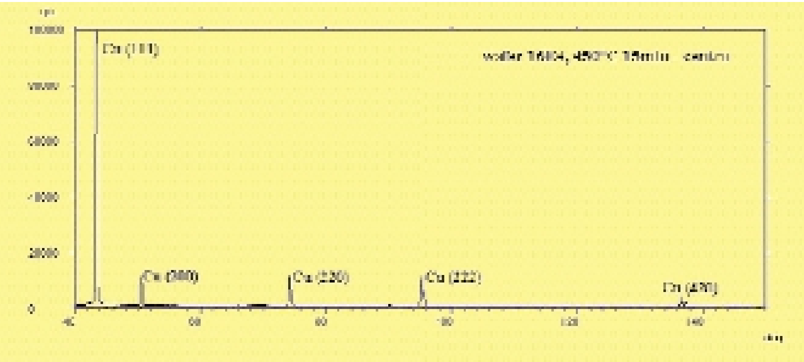
In Figure 11 two different diffractograms, one at 450°C and one of a self-annealed wafer, are reported for comparison. The XRD spectra show a slight difference even though the Cu (111) plane is dominant in both cases. Wafers without anneal and with low temperature (<200°C) anneal show a typical powder XRD pattern. This suggests that the Cu grains are very small in size and randomly oriented. There is no strong preferred crystal orientation in the self annealed Cu films as well as Cu films annealed at relatively low temperatures. As annealing temperature increases, however, X-ray diffraction from the Cu (111) plane becomes dominant. The XRD results are in good agreement with SEM image observation results in Figure 6. In order to better highlight any significant difference in terms of Cu planes, it should be necessary to treat the data in a different way, possibly by collecting the rocking curves of the Cu (111) plane.

Investigations in this direction will be done in future works.



a

(deg)	d (Å)	(I/Imax %)	
43,40	2,09	100	Cu (111), 43.30°
50,50	1,81	7	Cu (200), 50.43°
74,20	1,28	7	Cu (220), 74.13°
89,95	1,09	1	Cu (311), 89.93°
95,20	1,04	4	Cu (222), 95.14°
136,50	0,83	2	Cu (331), 136.51°
144,70	0,81	1	Cu (420), 144.71°



b

(deg)	d (Å)	(I/Imax %)	
43,40	2,09	100	Cu (111), 43.30°
50,55	1,81	3	Cu (200), 50.43°
74,20	1,28	3	Cu (220), 74.13°
95,20	1,04	3	Cu (222), 95.14°
136,55	0,83	1	Cu (331), 136.51°

Figure 11. XRD spectra of: a) 5.5 µm thick copper self-annealed wafer; b) 5.5 µm thick copper wafer annealed at 450°C for 15 minutes.

DISCUSSIONS

In terms of sheet resistance reduction of ECD Cu films, self annealing at room temperature for 8~24 hrs provides very repeatable results which are comparable to those (21~23% reduction in sheet resistance) obtained from Cu films annealed at higher temperatures (100~450°C) in forming gas ambient. No Cu grain growth during self-annealing at room temperature was observed. It's not easy to find a clear explanation of how the Cu self-anneal process reduces sheet resistance, though other authors [8] propose models to explain this phenomenon.

Devices using Cu interconnects often face reliability problems during normal operation due to the electromigration and/or stress migration of Cu atoms. Electromigration causes void formation (open circuit), which results in device failure. Performing a proper annealing before any further process step can reduce the risk of device failure. During device operation, device temperature rises substantially due to joule heating by electrical current. Joule heating and current flow through Cu interconnects enhances Cu atoms migration and Cu grain growth. By annealing Cu films properly, grains growth and film stress is released [8]. Coalition of small grains during grain growth reduces the aggregate of grain boundary surface area. As a result, the Cu film is densified. Once the Cu film is fully densified, Cu atoms are less mobile and are not able to migrate freely. Properly annealed Cu film may be less affected by electromigration, as well as stress migration, so significant improvement in device reliability can be expected after proper annealing. The authors are currently investigating the effect of Cu annealing in a forming gas atmosphere on device reliability, including electromigration tests.

When Cu film is annealed at elevated temperatures in mini environment with N_2 down flow, colour change of the Cu film due to oxidation was observed. This was due to high residual O_2 concentration in the annealing environment. The sheet resistance of the oxidised area was slightly higher than in the rest of the Cu film. To avoid oxidation, the residual O_2 level has to be controlled. Annealing in a forming gas (mixture of N_2 and H_2), as it is possible to do in the SAO, also helps reduce residual CuO formation.

CONCLUSION

A Cu annealing process was characterised using an ambient controlled, stacked hot plate-based annealing system in the temperature range of 100°C~450°C. The effect of annealing conditions on various thickness of Cu interconnects was investigated. Sheet resistance, uniformity, grain size and crystallographic orientation were measured as a function of annealing temperature, time and ambient. Sheet resistance was reduced by 21~23% from as deposited Cu films after annealing above 200°C for more than 2 min or above 100°C for more than 5 min. Significant Cu grain growth was observed in Cu films annealed above 300°C. The grain growth of up to 5.0µm was observed after annealing at 450°C. The grain size was preliminarily determined by annealing temperature. No correlation was observed between sheet resistance reduction and grain growth. The electrical and crystallographic characteristics of Cu films annealed using the hot plate-based annealing system were compared with self-annealed Cu films. A production worthy Cu annealing process was developed using the hot plate-based stacked annealing system. The process window for Cu annealing was found to be very wide.

Cu annealing using an ambient controlled, stacked hot plate-based annealing system was found to be very useful from the viewpoint of precise process control and reduction in device fabrication cycle time. Lot size flexibility and single wafer signature that the stacked hot plate-based annealing system (SAO–150/200LP) provided, were very convenient features for process development using a small lot size. Reasonable productivity (25 wph for 5 min process under residual O_2 concentration <5 ppm) with minimum facility requirements makes the transition to mass production easier when using this system.

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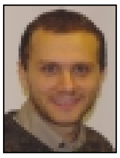

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