

HOT PLATES

DESPITE SINGLE WAFER BATCHES BECOMING THE NORM FOR 300MM, THERE ARE STILL APPLICATIONS WHERE MULTI BATCH PROCESSES ARE EFFECTIVE. **WOO SIK YOO AND TAKASHI FUKADA** OF WAFERMASTERS AND **JIRO YAMAMOTO** OF NEC HIROSHIMA DISCUSS A METHOD THAT ENABLES FIVE WAFERS TO BE PRODUCTIVELY ANNEALED AT LOW TEMPERATURES

A five wafer batch annealing system using resistively heated, stacked hot plates has been designed and tested for low temperature (100~450°C) annealing applications for 200mm and 300mm wafers. The system was designed to process five wafers simultaneously. This feature allows gradual heating of wafers required for low temperature annealing/baking applications without deteriorating productivity. Thermal properties of the five wafer batch annealing system and wafer temperature profiles during low temperature annealing in stacked hot plates were characterised as a function of hot plate temperature. The stacked hot plate configuration makes convection between hot plates negligible and provides a nearly isothermal environment for the wafer. As an example of process applications, spin-on-glass (SOG) annealing results were described.

Low temperature annealing is traditionally done in large batch furnaces. A typical batch size ranges from 150 to 200 wafers. As demand in small quantity production increases, the flexibility in lot size and reduction of cycle time becomes more important than ever. For those reasons, single wafer processing is essential for 300mm wafer processing applications. Cycle time reduction and risk reduction of large batch loss can be achieved by implementing single wafer processing. For relatively high temperature thermal processing applications above 600°C, lamp-heated single wafer RTP systems are frequently used. Accurate and reliable wafer temperature measurement/control below 600°C using optical pyrometry is difficult due to transparent optical property of Si in the IR region. This makes the lamp-heated single wafer RTP system difficult for low temperature thermal processing applications below 600°C. In addition, degradation of lamps and out gassing during annealing causes process pattern shift. This makes process control even more difficult. A new concept annealing system with the lot size flexibility and reduced cycle time needs to be developed for low temperature annealing applications up to 600°C.

To look at this issue a resistively heated, stacked hot plate system was proposed for low temperature annealing applications in the temperature range of 100~450°C. Typical applications of the system include SOG anneal, Cu anneal, Al anneal, low k dielectrics anneal and photoresist bake/reflow.

Heat Transfer Modes

Heat transfer is energy in transit due to a temperature difference. There are three heat transfer processes (or modes). They are conduction, convection and thermal radiation modes. Conduction takes place across the media (i.e. solid, liquid and gas). Convection occurs between a surface and a moving fluid (i.e. liquid and gas) when they are at different temperatures. The third mode is thermal radiation. Thermal radiation is the net heat transfer between surfaces in the form of electromagnetic waves in the absence of an intervening medium.

Si has a bandgap energy of 1.1eV and it only absorbs photons with higher energy than the bandgap. The absorption edge of Si is located around 0.96 μm ~1.2 μm in wavelength depending on doping level. Si is optically transparent in the IR region. As Si temperature increases, concentration of thermally generated carriers (i.e. electron-hole pairs) increases exponentially. Si becomes optically opaque in the IR region around 600°C. The radiation heat transfer is negligible when Si temperature is far below 600°C and wavelength from heat source is longer than the absorption edge of Si (0.96~1.2 μm). The wavelength of visible light is between 0.4 μm ~0.7 μm . Figure 1 shows the absorption coefficient of Si and light intensity distribution of a tungsten halogen lamp at different filament temperatures. As seen in figure 1, light energy from tungsten halogen lamps cannot be effectively absorbed by a Si wafer. Energy efficiency in wafer heating will be extremely poor. This fact has been well proven in lamp-based RTP systems.

For low temperature annealing applications below 600°C, the main heat transfer modes have to be conduction and convection.

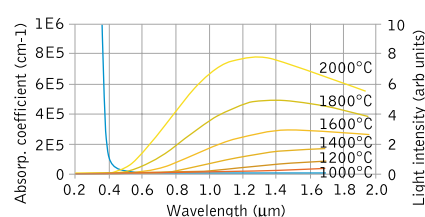


Fig. 1: Spectral absorption coefficient of Si and light intensity distribution of tungsten halogen lamp at different filament temperature

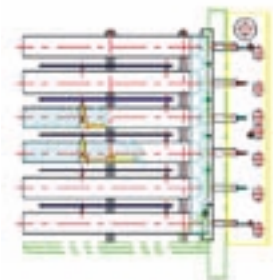
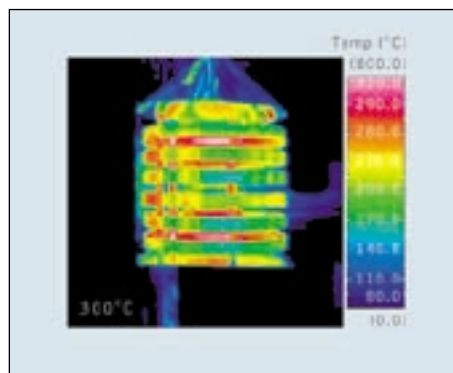


Fig. 2: Schematic diagram of stacked hot plates (a) and thermal image of the hot plates at 300°C

Conventional batch furnaces utilise the two heat transfer modes for wafer heating in temperatures below 800°C. Contribution in wafer heating from the radiation mode becomes a significant factor above 800°C.

Batch annealing oven

A resistively heated, stacked hot plate system was designed and tested for low temperature annealing applications in the temperature range of 100~ 450°C. This stacked hot plate system was designed to provide single wafer signature, lot size flexibility and reasonable productivity at a minimum facility requirement. Resistively heated hot plates were used to heat 200mm and 300mm Si wafers in this study. Figure 2 shows a side view of stacked hot plates with five Si wafers. The system was designed to process five wafers simultaneously. This feature allows the gradual heating of wafers required for low temperature annealing/baking applications without productivity deteriorating. The individual hot plate is made of aluminium with an embedded heater for temperature control. The aluminium was chosen as the hot plate material because of its thermal stability in the temperature range up to 450°C, high thermal conductivity and ease of machining. The hot plate is slightly larger than the Si wafer in diameter and significantly thicker (30mm) than the Si wafer. Individual hot plates have three standoffs to keep the distance between a wafer and the hot plate. The standoffs are equally spaced on the perimeter of approximately 70% of wafer diameter. The gap between the hot plates is 20mm. During the process, wafers are placed on standoffs on the bottom hot plate. The wafers are located in the middle of the top and bottom hot plates (10mm above the bottom hot plate and 10mm below the bottom hot plate).

The temperature uniformity of the hot plates was found to be very good. High thermal conductivity of aluminium prevents temperature gradation across the hot plates occurring. The thermal conductivity of gases is three to four orders of magnitude lower than that of aluminium. The poor thermal conductivity of gases makes heat dissipation through the gas conduction phase smaller. The stacked hot plate configuration makes convection between hot plates negligible and provides a nearly isothermal environment for the wafer. Wafer temperature profiles were investigated as a function of hot plate configuration, standoff height, hot plate temperature and process atmosphere [figure 2]

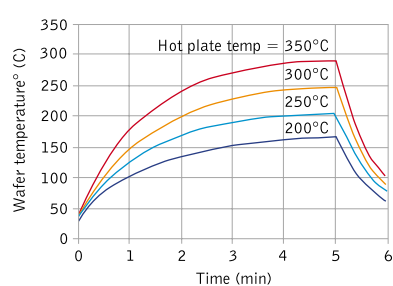


Fig. 3: Wafer temperature profiles during process under 1 atm air

300mm bare Si wafers with instrumentation thermocouples were annealed in the stacked hot plates at different temperatures under 1 atm air and He. The temperature of the six hot plates was controlled individually, but the temperature set points were kept the same. The wafer was placed on 8mm tall standoffs on the bottom hot plate. Temperature profiles on the wafer in stacked hot plates were measured at hot plate temperature set points of 200, 250, 300 and 350°C. Figure 3 shows the wafer temperature ramp up and ramp down profiles in the stacked hot plates.

As the wafer is inserted into the stacked hot plates, the wafer temperature initially increases gradually and then it saturates at little below the hot plate temperatures. Since the conduction heat transfer is one of the major heat transfer mechanisms at 1 atm air, the wafer temperature, ramp, up/down profile depends on ambient gas. When a high thermal conductivity gas such as H₂ or He is used as an ambient gas, the wafer temperature ramp rate and the saturated wafer temperature are higher than air, N₂, O₂ and Ar. The heat transfer between the hot plates and the wafer is predominated by thermal conduction through the gas. The thermal conductivity of air and He gas at 300K under 760Torr are 26.2x10⁻⁵ and 156.7x10⁻⁵ W/cmK, respectively. [1] The thermal conductivity of gases increases with temperature. The thermal conductivity of air and He gas become 45.7x10⁻⁵ and 252.4x 10⁵ W/cmK at 600K under 760Torr. [1] Wafer temperature ramp rate varies with the hot plate temperature, standoff height, process pressure and process atmosphere.

The direct contact between a wafer and a hot plate provides fast wafer temperature ramp up, but it results in non-uniform wafer heating during temperature ramp up. When wafers with films deposited or coated at low temperatures are directly placed on hot plates they tend to slide during annealing. This is due to the air bearing effect of out gassed species. By keeping an intentional gap between the hot plates and the wafer, good wafer temperature uniformity can be obtained throughout the process. Wafer sliding can also be prevented. The wafer temperature profiles suggest that non-contact thermal annealing is gentle and provides repeatable process results. Near warpage- free thermal annealing is achieved by placing a wafer on standoffs in stacked hot plates [figure 2]. A stacked hot plate system is very promising for wafer warpage

sensitive and out gassing low temperature annealing processes such as Cu anneal, Al anneal, SOG anneal, and photoresist baking applications [figure 3]

SOG Process Results

SOG annealing was carried out using the stacked hot plate annealing system. Changes in physical properties of SOG films before and after anneal were characterized as a function of temperature and time. Organic SOG films on 200mm Si wafers with an as-spun thickness of 360nm were under 1 atm air. The SOG film shrunk up to 18–19% when it was fully out gassed. The annealing temperature was varied from 200°C to 400°C. The annealing time was also varied between one and five minutes. The film thickness shrinkage and refractive index change after annealing under different conditions were measured. Figure 4 shows the surface response plots of film shrinkage and uniformity after annealing under various process temperature and time. As annealing temperature and time increase, thickness shrinks more and refractive index decreases due to the film densification. Thickness shrinkage up to 19% was obtained. Average thickness uniformity of SOG films after annealing ranges from 0.5 to 1.5% in 1σ .

Complete out-gassing that does not generate cracks in SOG films is desirable. To achieve this process goal, uniform and gradual heating of Si wafers for a relatively long time (four to five minutes) is desirable. Incomplete or nonuniform baking results in poor uniformity in etch rate selectivity in the following etch back process step. We were able to control SOG film properties using the batch annealing oven in the wide range of process conditions. Due to the five wafer simultaneous processing capability and gentle wafer temperature ramp up characteristics of the system, we were able to achieve very repeatable process results at higher productivity compared to conventional single hot plates and batch furnaces. Lot size flexibility was also improved compared to the batch furnaces without productivity deteriorating. Typical throughput for a three to five minute process is 60–40wph. While throughput is maintained to a comparable level in conventional large batch furnaces, we were able to reduce wafer cycle time significantly and improved the lot size flexibility. The throughput and process results (i.e. uniformity and repeatability) were excellent compared with conventional single hot plates.

Figure 5 shows a schematic diagram of a stacked annealing system for 300mm wafers. The system dimension is 1050mm (W) x 1600mm (D) x 2000mm (H) including two FOUP openers. The system operates under 1 atm air and does not require any process gas, compressed air or cooling water. Average power consumption is less than 6kW at 400°C operation. The system provides lot size flexibility as well as productivity. Throughput of the 300mm system is slightly lower than that of 200mm system because of FOUP opener operation. Throughput of 45wph and 35wph were achieved for 3min and 5min annealing processes, respectively.

The low temperature batch annealing system, employing six stacked hot plates, showed very promising test results in various low temperature annealing processes. It was also promising for low temperature annealing applications in GaAs and InP device fabrication processes. Chamber enclosure, process gases, vacuum pump and pressure control functions can be added for processes that require precise environmental control.

Conclusion

A five wafer batch annealing system using resistively heated, stacked hot plates was designed and tested for low temperature annealing of 200mm and 300mm wafers. The system is designed to process five wafers simultaneously in gradual heating environment that is suitable for low temperature annealing/baking applications without deteriorating productivity. Thermal properties of the annealing system and wafer temperature profiles during low temperature annealing in stacked hot plates were characterized as a function of hot plate temperature. The stacked hot plate configuration makes convection between hot plates negligible and provides nearly isothermal environment for the wafer. SOG films were annealed in the batch annealing oven. Changes in physical properties of SOG films before and after anneal was characterized as a function of temperature and time. Productivity and lot size flexibility of batch annealing oven are compared with conventional hot plates and furnaces. The low temperature annealing system which employs stacked hot plates is found out to be very promising for low temperature annealing processes such as Cu anneal, Al anneal, low k dielectrics anneal, and photoresist baking applications.

This article can be viewed on our website.

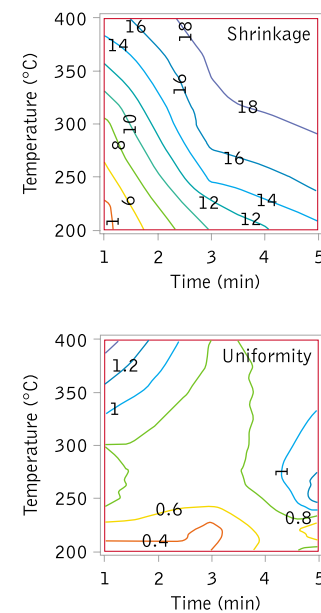


Fig. 4: Surface response plot of film shrinkage and uniformity after annealing under various process temperature and time

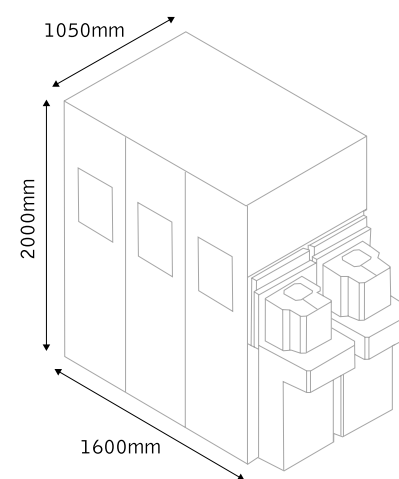


Fig. 5: Schematic diagram of 300mm batch annealing oven with two FOUP openers

U.S.A. **WaferMasters, Inc.**
246 East Gish Road
San Jose, CA 95112
Phone +1-408-451-0850
Fax +1-408-451-9729
<http://www.wafermasters.com>

Japan **WaferMasters Japan K.K.**
5-6-3-C Yanagibashi
Yamato, Kanagawa, 242-0022, Japan
Phone+81-46-268-6275
Fax+81-46-268-6293

Europe **WaferMasters, Inc. - Europe Operations**

