CHARACTERIZATION OF ULTRA-SHALLOW IMPLANTED P^+ LAYER ON P-TYPE SILICON SUBSTRATES AFTER FLASH ANNEAL AND CONVENTIONAL RAPID THERMAL ANNEAL

Tadashi Suzuki[1*], Masatoshi Seto[1], Norio Suzuki[1], Kitaek Kang[2] and Woo Sik Yoo[2]

[1]Trecenti Technologies, Inc., 751 Horiguchi, Hitachinaka, Ibaraki 312-0034, Japan
[2]WaferMasters, Inc., 246 East Gish Road, San Jose, CA 95112, U.S.A.

Electrical activation and dopant diffusion behavior of ultra-shallow B and BF_2 implanted p-type silicon wafers with various implant energies and dosages were studied before and after a novel millisecond flash anneal and a conventional tungsten halogen lamp-based rapid thermal anneal (RTA). Sheet resistance of implanted wafers was measured using a four point probe and B depth profiles were measured using secondary ion mass spectroscopy (SIMS) before and after annealing. Depth profiles of resistivity were also measured by using the spreading resistance profiling (SRP) method. SIMS depth profiles and resistivity profiles from SRP were compared. Flash annealing was found to be very effective in achieving nearly diffusion-free activation of ultra-shallow implanted layers with or without pre-amorphization implantation (PAI) of Ge.

INTRODUCTION

For ultra-shallow junction (USJ) formation beyond the 90 nm node, a short time annealing at high temperature with very fast ramp up (~250°C/s) and cool down rates (~150°C/s) using tungsten halogen lamp-based rapid thermal annealing (RTA) systems has been a very popular approach [1-3]. Annealing times at the peak temperature are often less than 1 s and this annealing method is often referred as "spike" anneal. In recent years, excimer laser-based and non-filament based arc lamp annealing techniques are being actively investigated due to their fast energy generation characteristics [4-13]. The photon generation times for the excimer laser and arc lamp are in the range of ns and ms, respectively. Solid phase epitaxy (SPE) at lower temperatures (<700°C) after USJ implantation is also examined by several research groups [14]. Plasma doping and epitaxial chemical vapor deposition (CVD) growth of highly doped layers are also being investigated as alternate doping methods for USJ formation [15-18].

To extend current ion implantation and annealing technology, a very rapid anneal (<10 ms) at a very high temperature (>1100°C) is considered to be the most promising method for USJ formation. A very short time surface heating is desired to electrically activate the dopant species without causing diffusion from heating the bulk Si wafer. Plasma doping with flash anneal is also proposed as one of the potential solutions. The precise control of the implant dosage and profile utilizing proper annealing methodologies must be established to achieve desired USJ formation. Due to the high diffusivity of boron (B) in Si, p-type USJ formation faces more difficult challenges than n-type (P or As based) formation.

In this study, $^{11}B^+$ (1.0 keV, 1.0 ~ 1.5 x 10^{15} ions/cm^2) and $^{49}BF_2^+$ (3.0 keV, 1.0 ~ 1.5 x 10^{15} ions/cm^2) implanted Si wafers were annealed using xenon arc-flash lamps or a conventional tungsten halogen lamp-based RTA system. Electrical activation and dopant diffusion behavior of ultra-shallow B and BF_2 implanted p-type silicon wafers were studied before and after a novel millisecond flash anneal and a conventional RTA. The effect of germanium (Ge) pre-amorphization implantation (PAI) was also studied.

EXPERIMENTAL

Proper characterization of ultra-shallow p^+/n junction is very difficult. Sheet resistance measurement using a four point probe is not reliable and often mischaracterizes the electrical properties of the active p^+ layer. Possible causes for the difficulties are: (1) too high resistance due to poor activation, (2) poor electrical isolation due to junction leakage, (3) punch-through of probes into n-type substrate, (4) non-uniform dopant profile, and (5) high concentration of electrically inactive dopants. For proper characterization of activated p^+ layer using a conventional four point probe, ultra-shallow p^+/p structures are fabricated instead. By employing the ultra-shallow p^+/p structures, junction leakage and punch-through related measurement problems can be eliminated.

To fabricate p^+/p structures, ^{11}B and $^{49}BF_2$ ions were implanted into p-type Si wafers with a resistivity of ~10 Ω·cm. at dosages and energies of $^{11}B^+$ (1.0 keV, 1.0 ~ 1.5 x 10^{15} ions/cm^2) and $^{49}BF_2^+$ (3.0 keV, 1.0 ~ 1.5 x 10^{15} ions/cm^2). For one set of wafers, ^{72}Ge was implantated (5.0 keV, 1.0 x 10^{15} ions/cm^2) to pre-amorphize the Si substrate prior to B or BF_2 ion implantation to achieve abrupt dopant profiles by reducing channeling effects. Another set of wafers was prepared without the Ge pre-amorphization. Wafers were annealed using either a conventional tungsten halogen lamp-based "spike" RTA system or a novel millisecond Xe arc lamp based flash annealing system.

Annealing characteristics of ultra-shallow B and BF_2 implanted p-type Si wafers with and without Ge pre-amorphization were investigated in terms of electrical activation and dopant redistribution after annealing. Boron, fluorine (F) and Ge depth profiles were measured using secondary ion mass spectroscopy (SIMS) before and after annealing. Sheet resistance of implanted wafers was measured using a four point probe and depth profiles of resistivity also measured by the spreading resistance profiling (SRP) method. B depth profiles from SIMS and SRP resistivity profiles were compared.

RESULTS AND DISCUSSIONS

For successful ultra-shallow p^+/p layer formation, both control of the as-implanted B depth profile and proper electrical activation of B with minimum diffusion are required. The effect of Ge pre-amorphization on as-implanted B profile abruptness has been reported [12]. To verify the effect, as-implanted B, F and Ge depth profiles were measured using SIMS as the reference. Figure 1 summarizes the B depth profiles of B and BF2 implanted wafers, with and without Ge pre-amorphization implantation. BF_2

implanted at 3.0 keV implanted wafers had more shallow as-implanted B depth profiles than B 1.0 keV implanted wafers, regardless of Ge pre-amorphization. The Ge pre-amorphization was found to be very effective in reducing the channeling effect during subsequent B or BF_2 implantations resulting in a 2~3 times steeper B depth profile than regular B or BF_2 implanted wafers. The Ge pre-amorphization appears very promising for making abrupt dopant profiles with results being very consistent with previously reported results [12]. When Ge implantation is used for pre-amorphization, the effect of Ge in Si has to be considered. With Ge implantation conditions of 5.0 keV, 1.0×10^{15} cm^{-2}, a heavily Ge implanted region with a Ge concentration maximum of ~ 1.0×10^{22} atoms/cm^3 is formed 2~3 nm below the surface. Thus, Ge concentration in this region is almost 20 atomic percent that of Si. As seen in SiGe alloys, with the large amount of Ge incorporation, up to 1.0×10^{22} atoms/cm^3 near the surface, there is a reduction of the Si bandgap and enhanced UV absorption characteristics. The impact of the high concentration Ge atoms near the surface must be carefully evaluated in interpreting electrical characterization results.

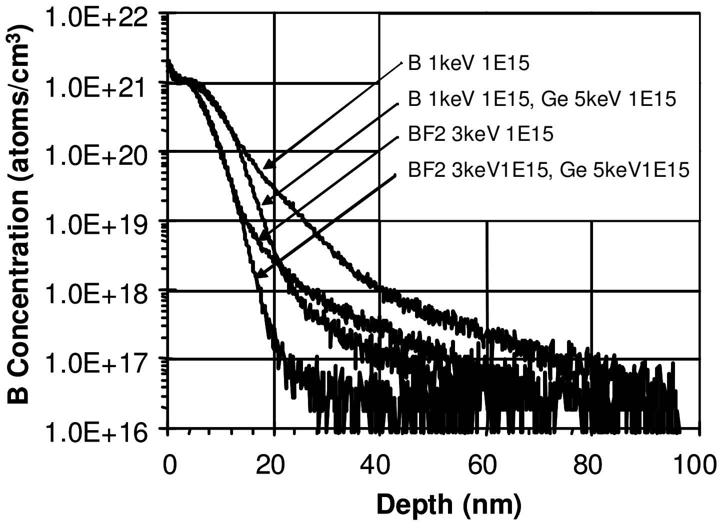

Figure 1. As-implanted B depth profiles under various implant conditions.

SIMS depth profiles of ^{11}B (1.0 keV, 1.0×10^{15} cm^{-2}) with Ge (5.0 keV, 1.0×10^{15} cm^{-2}) pre-amorphization implanted wafers before and after different annealing conditions are shown in Fig. 2. The as-implanted depth of B concentration at 1.0×10^{18} cm^{-3} was 22 nm. In all flash annealed wafers with preheating temperature below 500^{o}C, the change of the B profile is negligible with almost no dopant diffusion observed. The electrical activation of B implanted silicon was improved as flash power or pre-heating temperature was increased without causing B diffusion. The sheet resistance of wafers annealed with flash energy levels of 80% and 100% was measured as 98.97 ohm/sq. and 98.69 ohm/sq., respectively. Wafers annealed by conventional tungsten halogen lamp-based "spike" rapid thermal anneal (RTA) at 1050^{o}C showed electrical activation however a significant B diffusion with the sheet resistance measured as 94.97 ohm/sq. After the "spike" anneal, the depth of B concentration at 1.0×10^{18} cm^{-3} was increased to 49 nm, an increase of 27 nm. Flash anneal was very effective in nearly diffusion-free activation of ultra-shallow implanted layers with or without Ge PAI.

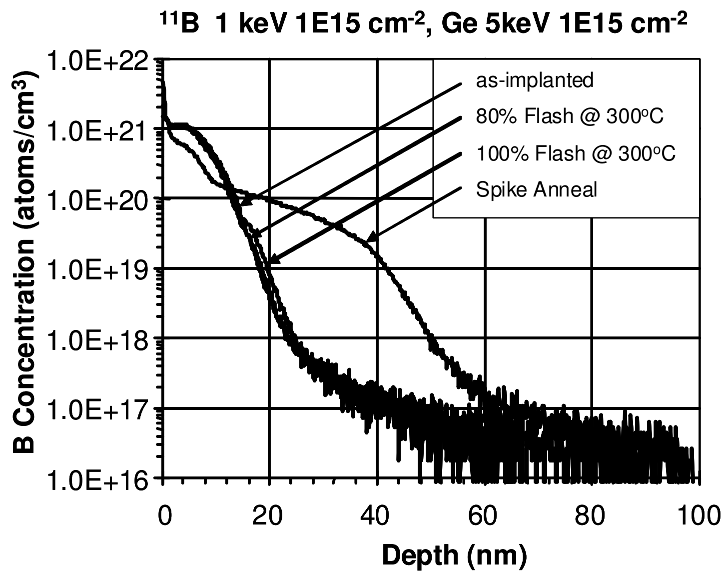

Figure 2. SIMS depth profiles of ^{11}B implanted wafers before and after different annealing conditions.

Figure 3 (a) and (b) show SIMS depth profiles of B and F atoms of $^{49}BF_2$ (3.0 keV, 1.0 x 10^{15} cm^{-2}) with Ge (5.0 keV, 1.0 x 10^{15} cm^{-2}) pre-amorphization implanted wafers before and after annealing. As-implanted depth of B concentration at 1.0 x 10^{18} cm^{-3} was 18 nm (Fig. 3 (a)). The depth was increased by 2 nm after flashing with a 100% rated power of flash annealing system and a preheating temperature of 300°C. The sheet resistance of wafers annealed with 80% (0.4 MJ) and 100% (0.5 MJ) of flash energy was measured as 459.45 ohm/sq. and 118.39 ohm/sq., respectively. A significant sheet resistance drop was observed between 80% and 100% power flashes. In contrast, the "spike" anneal increased the depth of B concentration at 1.0 x 10^{18} cm^{-3} to 38 nm, a depth increase of 20 nm. The sheet resistance was measured as 107.57 ohm/sq. All wafers showed F loss after annealing (Fig. 3 (b)). Fluorine atoms behaved quite differently than B atoms when using the flash anneal. Flash annealed wafers at a preheating temperature of 300°C showed 8% and 15% F loss with a majority of F atoms remaining even after the flash anneal. One small F concentration peak of low to mid 10^{18} cm^{-3} was developed around 17 nm from the surface. As the flash power increases, F loss increases. In contrast, almost all (97.3%) F atoms were removed after the "spike" anneal. It seems that there is some interaction between electrical activation and F loss. Both $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers, with and without Ge pre-amorphization, showed very similar electrical activation and dopant diffusion behaviors. Since the Ge PAI wafers showed more abrupt B depth profiles before annealing, dopant activation results from Ge PAI wafers are mainly discussed in this paper.

SIMS dopant profiles only gives total dopant concentration at a given depth regardless of the level of electrical activation of dopants. In order to characterize active carrier concentration profiles, SRP measurements were performed. A depth resolution of 2.5 nm/step was achieved by using 800:1 beveled specimens with a 2 µm step. Typical accuracy of the depth scales and carrier concentration estimation are ±3% and ±20%.

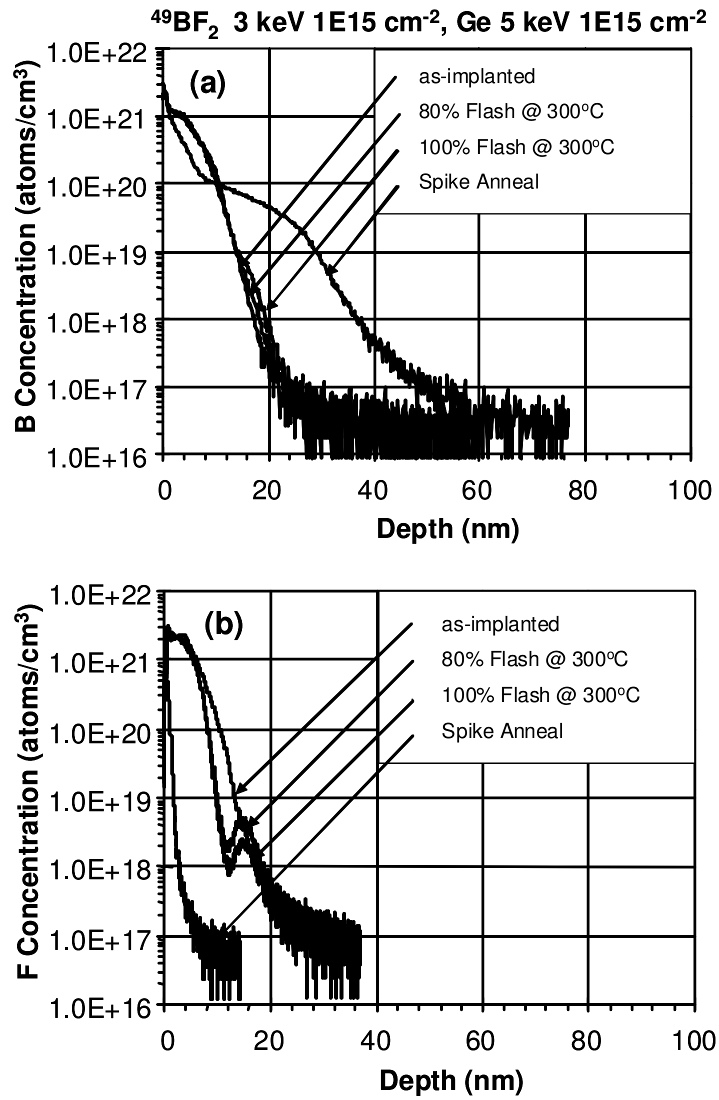

Figure 3. SIMS depth profiles of (a) B and (b) F of BF_2 implanted wafers before and after annealing.

When a high concentration of inactive dopants is present, considerable measurement distortion makes the carrier concentration estimation difficult and inaccurate. The heavily doped silicon as a result of shallow ion implantation and annealing greatly limits the activation due to the practical limitations of time at the required annealing temperatures. It is reasonable to assume that there are high concentrations of inactive dopants in the ion implanted layer even after annealing. In fact, we have observed the anomalous distortions of measurement influenced by inactive dopants' charges in a number of measurements. However, the SRP plots are effective in qualitatively determining the activation levels of heavily implanted shallow layers under various annealing conditions.

Electrically active carrier concentration profiles of ^{11}B (1.0 keV, 1.0 x 10^{15} cm^{-2}) with Ge (5.0 keV, 1.0 x 10^{15} cm^{-2}) pre-amorphization implanted wafers under the "spike" anneal and various flash anneal conditions were estimated using SRP measurement data shown in Fig. 4. For flash annealed wafers, a fixed flash power (100% of system rating) was applied with different preheating temperatures. Since the resistivity of Si wafers used in this study was in the range of ~10 Ω·cm, a background carrier concentration of ~1.0 x 10^{15} cm^{-3} is expected. As seen in the Fig. 4, the background carrier concentrations of all the wafers were in the range of ~1.0 x 10^{15} cm^{-3}. The "spike" annealed wafers showed significant dopant diffusion from the as-implanted profile. As shown in Fig. 2, after the "spike" anneal, the depth of B concentration at 1.0 x 10^{18} cm^{-3} was increased from 22 nm to 49 nm. The carrier concentration profiles of Fig. 4 shows a drop to the background level of ~1.0 x 10^{15} cm^{-3} at a depth of 50 nm from the surface. However, the flash annealed wafers showed very clear correlation between the electrical activation level (carrier concentration and activated depth) and preheating temperature under the same flash power. As the preheating temperature increases, the activation was enhanced without dopant diffusion.

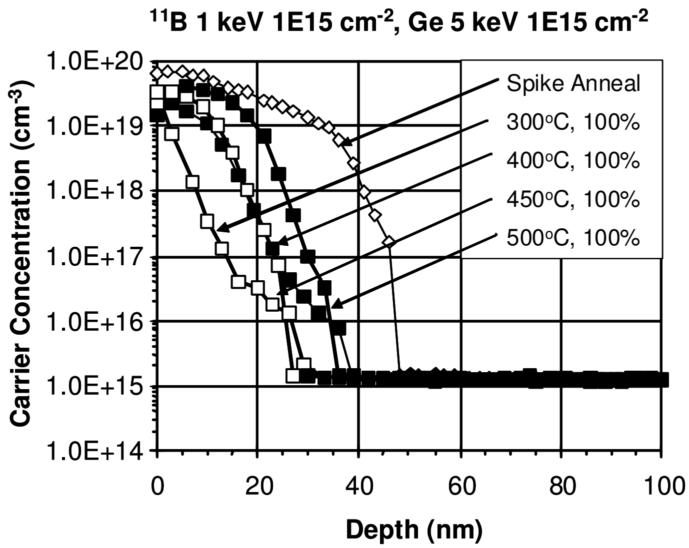

Figure 4. Active carrier concentration profiles of ^{11}B implanted wafers after annealing under various conditions.

Figure 5 shows electrically active carrier concentration profiles of $^{49}BF_2$ (3.0 keV, 1.0 x 10^{15} cm^{-2}) with Ge (5.0 keV, 1.0 x 10^{15} cm^{-2}) pre-amorphized implanted wafers using the "spike" anneal and various flash anneal conditions. For flash annealed wafers, two different flash power at 80% and 90% of system rating were applied with two different preheating temperatures of 300°C and 500°C. As noted, the "spike" annealed wafers showed significant dopant diffusion from the as-implanted profile. After the "spike" anneal, the depth of B concentration at 1.0 x 10^{18} cm^{-3} was increased from 22 nm to 50 nm (Fig. 3 (a)). The carrier concentration was also dropped down to the background level of ~1.0 x 10^{15} cm^{-3} at a depth around 42 nm from the surface. For flash annealed wafers, a higher flash power resulted in higher electrical activation and similar results are observed for higher preheating temperatures.

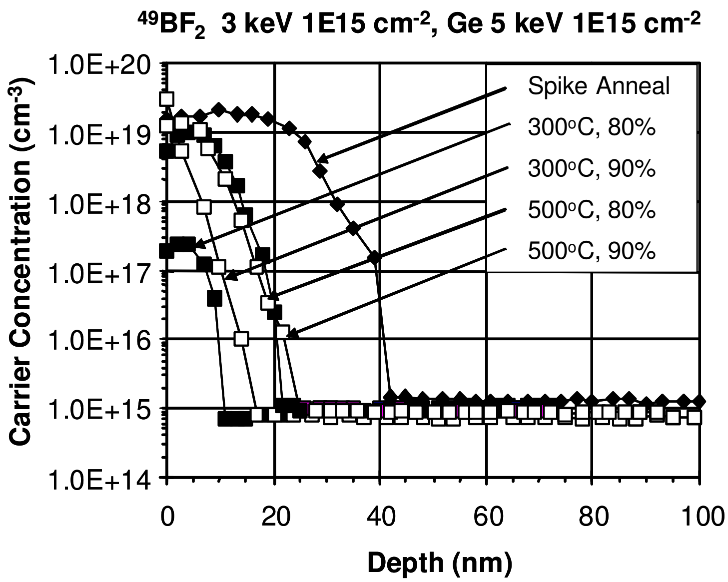

Figure 5. Active carrier concentration profiles of $^{49}BF_2$ implanted wafers after annealing under various conditions.

It was confirmed that the change in B SIMS profile of all flash annealed wafers with preheating temperature below 500°C was negligible with nearly no dopant diffusion observed. The electrical activation of B implanted silicon was improved as flash power or pre-heating temperature was increased also without B diffusion occurring. The increase of flash power or preheating temperature results in the increase of peak temperature of the wafer surface during the flash and the higher peak temperature of wafer surface, provides higher electrical activation. However, the maximum peak temperature of the wafer surface has to be optimized by selecting the proper preheating temperature and flash power based on ion implantation conditions. When the preheating temperature is too high, for example 800°C, the cool down rate of wafer surface becomes slower and results in significant dopant diffusion even in milliseconds [11-12].

SUMMARY

Electrical activation and dopant diffusion behavior of ultra-shallow B and BF_2 implanted p-type silicon wafers were studied before and after a novel millisecond flash anneal and a conventional tungsten halogen lamp-based RTA. Implant species, energies and dosages were varied and the effect of Ge PAI on as-implanted B profiles and electrical activation efficiency was investigated. Sheet resistance of implanted layers before and after annealing was measured using a four point probe. Depth profiles of resistivity were also measured by SRP method and giving an estimated depth profile of carrier concentration. B depth profiles were measured using SIMS before and after annealing and were compared with carrier concentration profiles from SRP to estimate the activation rate of dopants. The electrically active carrier concentration of all wafers regardless of annealing methods ("spike" anneal or flash anneal) is estimated to be far less than few percent of B concentration near the wafer surface. Since the boron solid solubility and diffusivity in Si are strongly affected by the Si temperature, a high power, millisecond flash anneal is demonstrated to be very effective in electrical activation of fast diffusing dopants such as B without significant diffusion. The millisecond flash anneal is promising in forming ultra-shallow junctions for advanced device applications.

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keywords

1. ultra-shallow implant

2. xenon arc lamp

3. flash anneal

4. electrical activation

5. dopant diffusion

NAME: WOO SIK YOO

Affiliation: WaferMasters, Inc.

Address: 246 East Gish Road

City/ Zip code: San Jose, CA 95112

Country: U.S.A.

Email: woosik.yoo@wafermasters.com

Phone : +1-408-451-0850