SIGNIFICANT IMPROVEMENT IN DEVICE PERFORMANCE OF ADVANCED DYNAMIC RANDOM ACCESS MEMORY BY HOT WALL-BASED SINGLE WAFER RAPID THERMAL ANNEALING

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To overcome the difficulties in lamp-based, cold wall rapid thermal processing (RTP) systems, a comparative annealing study of several critical RTP process steps was performed using a hot wall-type single wafer rapid thermal furnace (SRTF) system. In the SRTF system, unlike cold wall-type (lamp-based) RTP systems, the wafer is the coldest object in the process chamber at all times. In mass production of 512 Mbit DRAM devices with 110 nm design rules, significant improvement in electrical characteristics such as channel resistance variation and charge holding time, was obtained by switching annealing steps from a lamp-based RTP system to a furnace-based SRTF system. The flatness of wafers after annealing in the SRTF system was also improved up to 50 times compared to those annealed using the lamp-based RTP systems.

INTRODUCTION

For advanced dynamic random access memory (DRAM) devices below 130nm design rules, the precise control of thermal budget is one of the key issues in thermal processing. Keeping the variation in device performance (within-wafer and wafer-to-wafer) low is very important from the device yield management and quality control point of view. With the shrinkage in device dimensions and allowable thermal budgets, lamp-based, single wafer rapid thermal processing (RTP) systems became very popular in limited thermal processing applications.

In a lamp-based RTP system (cold wall system), the wafer temperature is dynamically controlled using feedback signals from in situ pyrometric wafer temperature measurement. Precise wafer temperature measurement and control are still a significant technical challenge. It is difficult to maintain temperature uniformity during thermal processing. Local and global temperature repeatability are dependent on many factors, such as the emissivity distribution of the wafer, chamber wall temperature and chamber wall reflectivity. Frequent calibration and maintenance are required. For advanced DRAM applications, the temperature uniformity, temperature repeatability, emissivity dependency and pattern density effects of lamp-based RTP systems must be improved for adequate performance.

To overcome the difficulties in lamp-based, cold wall RTP systems, the authors performed a comparative annealing study of several critical RTP process steps using a hot wall-type single wafer rapid thermal furnace (SRTF) system. In the SRTF system, the wafer is the coldest object in the process chamber at all times, unlike cold wall-type, lamp-based RTP systems. As long as the process environment temperature is uniform and the thermal mass of the system is sufficiently large, local and global temperature uniformity within a wafer and wafer-to-wafer temperature repeatability did not present a problem in the SRTF system. In this case, temperature repeatability is less dependent on local and global emissivity distribution on the wafer because uniform heat is supplied from surroundings, primarily by convection and conduction through ambient gas.

In this paper, rapid thermal annealing (RTA) of various critical implant annealing steps was performed using a lamp-based RTP system and an SRTF system under 1 atm N_2 atmosphere to compare resulting sheet resistance and its uniformity after annealing. Process windows for the lamp-based conventional RTP and for the SRTF systems are also compared. Dopant depth profiles and thermally induced stress of annealed wafers were investigated using secondary ion mass spectroscopy (SIMS) and optical interferometry. Electrical performance of 512 Mbit DRAM devices with 110 nm design rules fabricated using both system types were characterized and compared.

EXPERIMENT

A lamp-based RTP system (cold wall system) and a furnace-based single wafer RTP system (hot wall system) were used in this study. The lamp-based RTA system employs arrays of tungsten halogen lamps and illuminates a Si wafer through the quartz process tube from top and bottom sides. Wafer temperatures are measured using a pyrometer through the quartz tube. A multiple zone power control method is used to adjust temperature uniformity on a Si wafer. Wafer temperature ramp up rate, soak time and ramp down rate are programmable.

The SRTF system with a vacuum loadlock is used as a hot wall RTP system. The system consists of vertically stacked process chambers (furnace), a vacuum loadlock and two cooling stations. The process tube has three standoffs made of quartz. The process tube uses no moving parts for simplicity and system reliability. The wafer is placed on the quartz standoffs in the middle of the quartz process tube. The distance between the wafer and the quartz walls is kept at ~10 mm for both upward and downward directions. The quartz process tube is located in a SiC cavity which acts as a heat distributor to create an isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly. The SiC cavity temperature is monitored and controlled at a predetermined process temperature by three embedded R-type thermocouples and a three zone heater assembly to provide a consistent and nearly isothermal environment to the wafers regardless of wafer type and condition. Detailed system configuration, thermal characteristics and process performance of the system has been reported elsewhere [1-2].

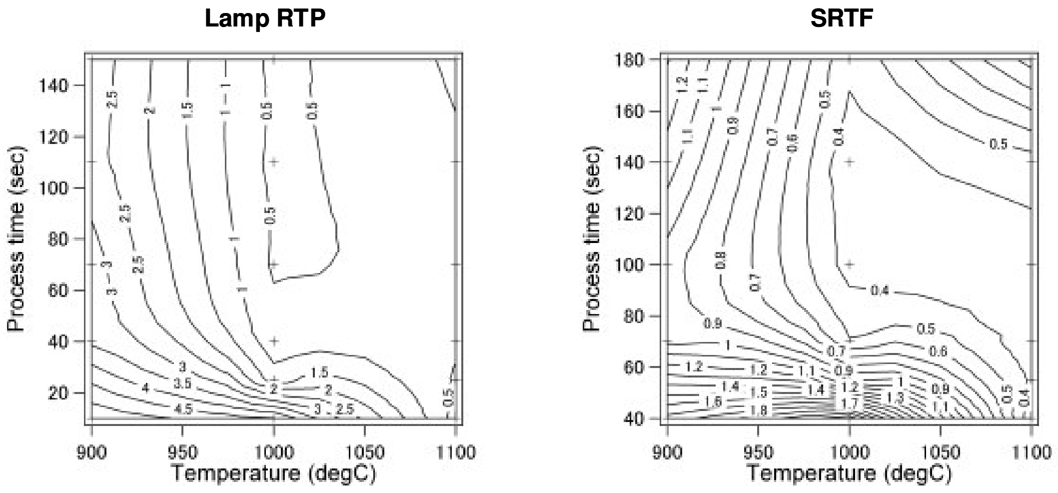
Implanted blanket and device wafers were annealed using both systems to investigate the effect of the annealing (heating) method on electrical activation of implanted species, dopant redistribution profiles, thermally induced stress (warpage) and device performance.

RESULTS AND DISCUSSIONS

Average sheet resistance and sheet resistance uniformity of four different types of implanted wafers ($^{11}B^+$ 50 keV $1x10^{15}$ cm^{-2}, $^{49}BF_2^+$ 70 keV $1x10^{15}$ cm^{-2}, $^{31}P^+$ 70 keV $1x10^{15}$ cm^{-2} and $^{75}As^+$ 70 keV $1x10^{15}$ cm^{-2}) were measured after RTA under various conditions using both the lamp-based RTP and SRTF systems. All four kind of implanted wafers were sufficiently electrically activated above 1000°C, independent of the wafer heating method (annealing system) used. Equivalent average sheet resistance values were achieved in wafers annealed using both systems. A higher temperature sensitivity of sheet resistance was observed in $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers compared to those in $^{31}P^+$ and $^{75}As^+$ implanted wafers.

The sheet resistance uniformity for all four different types of implanted wafers ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$) annealed at 900°C and 1000°C using the SRTF system were below 1.0% (1σ). $^{49}BF_2^+$ and $^{75}As^+$ implanted wafers showed slight increase of sheet resistance uniformity values after annealing at 1100°C, while the average sheet resistance value remain constant. In the case of the lamp-based RTP system, all four types of implanted wafers ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$ and $^{75}As^+$) annealed at 1000°C had measured sheet resistance uniformity below 1.0% (1σ) [3-4]. At annealing temperatures of 900°C and 1100°C, sheet resistance uniformity values of most implanted wafers exceeded 1.0% (1σ). In case of $^{49}BF_2^+$ implanted wafers, both average sheet resistance and its uniformity values significantly increased after annealing at 1100°C. The average sheet resistance value was increased from 102.6 ohm/sq. at 1000°C to 146.4 ohm/sq. at 1100°C. The sheet resistance uniformity value in 1σ was also significantly increased from 0.25% (at 1000°C) to 10.22% (at 1100°C) after annealing [5].

The average sheet resistance and sheet resistance uniformity of $^{11}B^+$ (50 keV $1x10^{15}$ ions/cm^2) implanted wafers are shown in Figs. 1 (a) and (b) as a function of annealing temperature and time. As seen in the figures, behavior of the average sheet resistance and sheet resistance uniformity in annealed wafers are very complex. In wafers annealed using the SRTF system, sheet resistance decreases with increasing annealing temperature and annealing time due to electrical activation of implanted species. The sheet resistance values are very sensitive to annealing temperature in the temperature range of 900°C and 1000°C, regardless of the annealing system used. In terms of sheet resistance uniformity, the SRTF system provides a wide process window for annealing conditions [3-4]. In general, longer annealing at lower temperatures gives lower average sheet resistance and superior sheet resistance uniformity.



(a) (b)

Figure 1. Surface response maps of sheet resistance uniformity after $^{11}B^+$ (50 keV $1x10^{15}$ ions/cm^2) implant annealing in lamp-based RTP (a) and SRTF (b) systems.

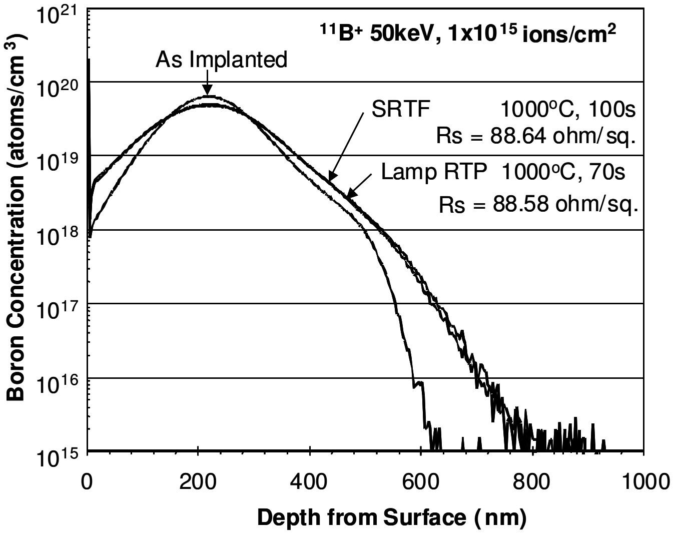
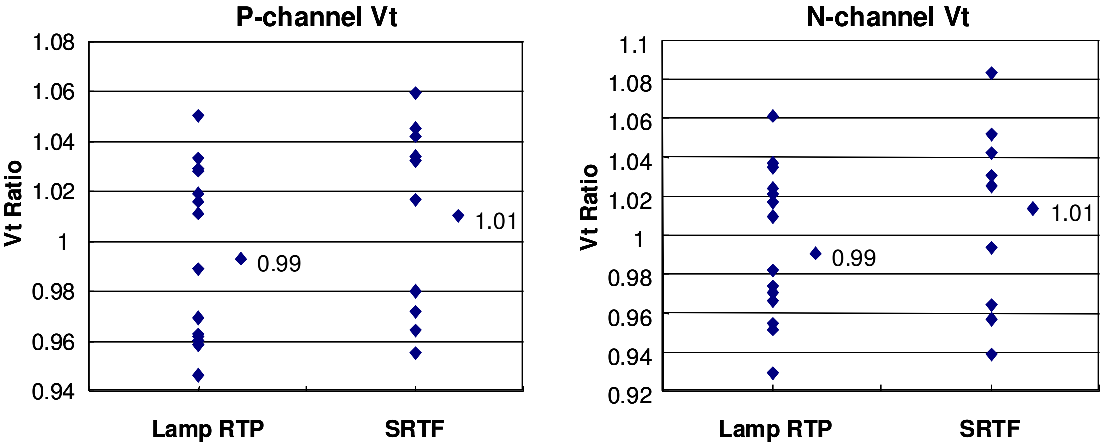


Figure 2. SIMS depth profiles of as implanted wafer and wafers after annealing in the lamp-based RTP and SRTF systems.

Figure 2 shows SIMS depth profiles of as implanted ($^{11}B^+$ 50 keV, $1x10^{15}$ ions/cm^2) wafer and wafers annealed at 1000°C in the lamp-based RTP and SRTF systems. Annealing times for the lamp-based RTP and SRTF systems were 100 s (wafer-in to wafer-out) and 70 s (soak time), respectively. Diffusion of boron atoms both the surface and deeper into the bulk was observed after annealing. Both average sheet resistance and SIMS depth profiles for wafers annealed using the different types of annealing systems were nearly identical.

Average sheet resistance and sheet resistance uniformity of blanket 200 mm diameter Si wafers implanted with various species after annealing were measured to optimize the annealing process. Annealing conditions for both systems were optimized and matched based on various implant anneal results. Typical sheet resistance uniformity after annealing was less than 1.0% in 1σ regardless of implant species and annealing system. After matching annealing conditions between the lamp-based RTP and SRTF systems, extensive split test was performed using 512 Mbit DRAM device wafers with 110 nm design rules. The n-channel and p-channel threshold voltage Vt ratios of devices annealed in the two RTP systems were plotted in Figs. 3 (a) and (b). Both n-channel and p-channel Vt ratios of actual devices were almost identical, independent of the annealing system used.

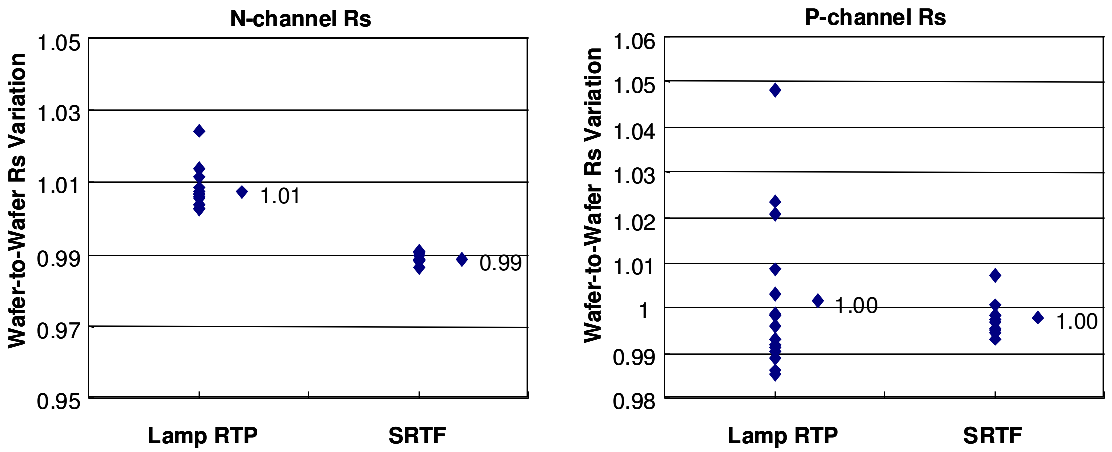


(a) (b)

Figure 3. N-channel (a) and p-channel (b) threshold voltage Vt ratios of DRAM devices annealed in lamp-based RTP and SRTF systems.

Figures 4 (a) and (b) show n-channel and p-channel wafer-to-wafer average sheet resistance variations of devices fabricated using in lamp-based RTP and SRTF systems. Wafer-to-wafer variation of average sheet resistance of n- and p-channel layers are almost 3 times larger in wafers annealed using the lamp-based RTP systems than for those annealed in the SRTF system. The furnace-based SRTF system always provides consistent results with the least amount of variation. As long as the implant uniformity is the same, the sheet resistance uniformity and repeatability is strongly dependant upon the uniformity and stability of the thermal environment in which the wafers are annealed. The wafer-to-wafer repeatability is strongly influenced by the stability of the system. The lamp-based RTP system operates as a cold wall-type system and lacks thermal stability.

The system always tries to control wafer temperature by adjusting lamp power based on imprecise wafer temperature measurements. Multiple zone temperature measurement and control make the control system complicated and process repeatability poor. Wafers are always processed under thermal transient conditions. In hot wall-type SRTF systems, wafers are processed stably, under near-thermal equilibrium conditions by controlling the temperature of the process environment instead of trying to control wafer temperature with imperfect and inconsistent measurement data. Thus, the hot wall-type system generally provides superior within-wafer uniformity and wafer-to-wafer process repeatability.



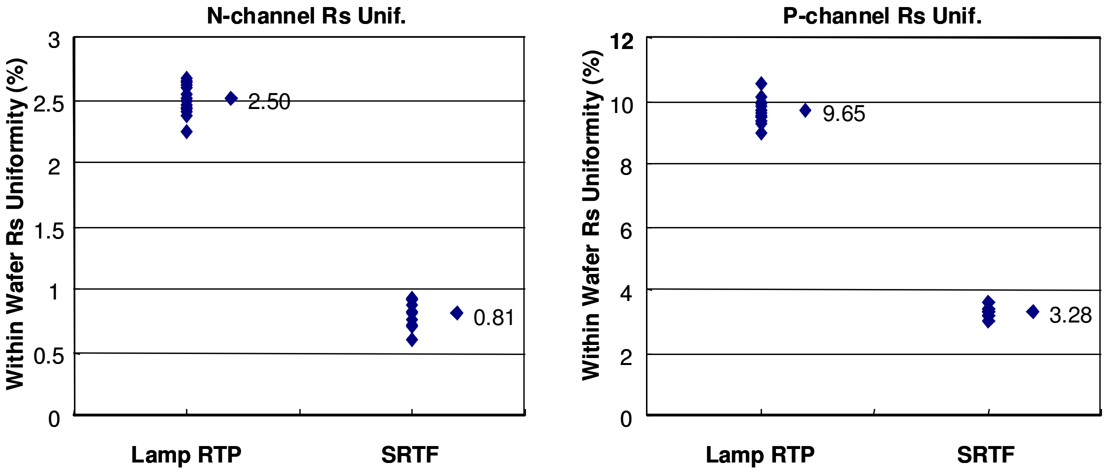
(a) (b)

Figure 4. N-channel (a) and p-channel (b) wafer-to-wafer average sheet resistance variations of DRAM devices annealed in lamp-based RTP and SRTF systems.

Within-wafer sheet resistance uniformity of n- and p-channel layers are plotted in Figs. 5 (a) and (b). P-channel sheet resistance uniformity was nearly 4 times larger than n-channel layers regardless of the annealing system. Using the SRTF system, sheet resistance uniformity for both n- and p-channel device wafers showed nearly a 3-fold improvement than those from device wafers annealed using the lamp-based RTP system. The furnace-based SRTF system provides superior within-wafer sheet resistance uniformity in both n- and p-channel device wafers.

This is because in the lamp-based RTP system, the wafer is the hottest object in the process chamber and it will naturally lose heat to the much colder chamber walls. Thus, it is very difficult to maintain temperature uniformity during the process. Temperature repeatability is also dependent on many factors such as the local and global emissivity distribution on the wafer, chamber wall temperature and wall reflectivity. When patterned wafers, such as device wafers are used, pattern induced temperature nonuniformity within a wafer becomes a serious problem [6-7]. The pattern density effect is more pronounced in radiation heating compared to conduction and convection heating. As long as radiation heating is the dominant heating mechanism, the pattern effect cannot be avoided. It is important to realize that the process results on device wafers are much different from the process results obtained on un-patterned blanket wafers. This large variation must be considered in device design.

In the SRTF system, a wafer is the coldest object in the process chamber at all times. As long as the temperature of the process environment is uniform and the thermal mass of the process chamber is sufficiently large, temperature uniformity within the wafer and temperature repeatability from wafer-to-wafer should not be a problem. The temperature repeatability is less dependent on local and global emissivity distribution on the wafer because uniform heat is supplied from surroundings mainly by conduction and convection. These mechanisms, and hence the process results, are less sensitive to pattern density on device wafers. For the SRTF, the process results on blanket wafers and device wafers are almost identical. When the SRTF system is used, the within-wafer process results can be tightly controlled regardless of wafer type and pattern density variation.



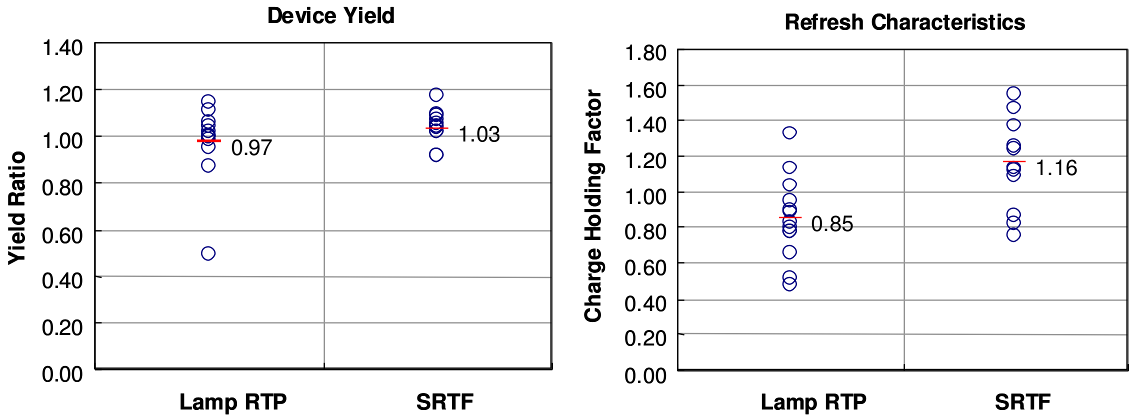
(a) (b)

Figure 5. N-channel (a) and p-channel (b) within-wafer sheet resistance variations of DRAM devices annealed in lamp-based RTP and SRTF systems.

Production yield and refresh characteristics of 512 Mbit DRAM devices annealed in the lamp-based RTP and SRTF systems are shown in Figs. 6 (a) and (b). The wafers processed using the SRTF system resulted in 6 percent improvement (from 0.97 to 1.03) in device yield in split-lot tests. Significant improvement (36% increase from 0.85 to 1.16) in charge holding characteristics was observed in devices fabricated using the SRTF system compared to ones fabricated using the lamp-based RTP system.

Since the n- and p-channel sheet resistance variation during RTP steps, using conventional (lamp-based) RTP systems, is already considered in the worst case scenario by chip designers, the decrease in sheet resistance variation generally does not affect the device yield ratio unless the sheet resistance of individual devices is near the yield critical value. In other words, the device yield can only be a good indicator if the process shift towards the yield critical value and cannot detect process quality improvement otherwise. To assess process quality improvement, electrical characteristics (such as charge holding factor in DRAM devices) of individual devices have to be measured. The 36% improvement in charge holding characteristics observed in devices fabricated using the SRTF system compared to those using the lamp-based RTP system indicates a reduction in leakage current from capacitor cells. DRAM devices fabricated using the SRTF system are more reliable and are less likely to fail. The authors are currently investigating the possible origin of the improvement seen in the charge holding characteristics. A preliminary investigation suggests that thermal stress on the wafers is the major source of leakage current increase (degradation of charge holding characteristics). The thermally induced wafer warpage was characterized after annealing using the both systems. The flatness of wafers from the SRTF system was up to 50 times better than those annealed using the lamp-based RTP systems. This is due to the “nearly” isothermal process environment of the SRTF system. The flat surface of the annealed wafers enables much better results in subsequent lithography steps which is an important advantage. Detailed investigation results will be reported separately.

By virtue of the low maintenance and calibration free system design features of the SRTF, equipment up time exceeded 99% over a one year period. The facility cost savings over lamp-based RTP system was more than 30%. Negligible consumable cost and spare parts costs were experienced over the one year period.



(a) (b)

Figure 6. Production yield (a) and refresh characteristics (b) of 512 Mbit DRAM devices annealed in lamp-based RTP and SRTF systems.

CONCLUSIONS

A comparative annealing study of several critical RTP process steps was performed using a conventional lamp-based, cold wall-type RTP system and a hot wall-type SRTF system in a 512Mbit DRAM mass production environment to overcome quality control difficulties due to large variations in die-to-die electrical properties in devices. The differentiation is that in the SRTF system, the wafer is the coldest object in the process chamber at all times and is controlled by a single, stable, large thermal mass. In cold wall-type, lamp-based RTP systems, the wafer temperature must be controlled by a large number of small, non-uniform heat sources directly heating the wafer surface.

In p- and n-channel devices, the standard deviation of resistance values within-wafer and from wafer-to-wafer, was one-third to one-half that from wafers annealed using the lamp-based RTP systems. When the SRTF system was used, the charge holding characteristics of DRAM cell transistors were also improved significantly (36%) due to the excellent local and global temperature uniformity on the wafer. Emissivity and pattern density effects were also negligible compared to those from the lamp-based RTP systems. The flatness of wafers after annealing in the SRTF system was improved up to 50 times compared to those annealed using the lamp-based RTP systems.

In mass production of 512 Mbit DRAM devices using 110 nm design rules, significant improvement in electrical characteristics, such as channel resistance variation and charge holding time was obtained by switching annealing steps from a lamp-based RTP system to the furnace-based SRTF system. The “nearly” isothermal process environment of the SRTF system and the flat surface of the annealed wafers also provide better results in subsequent lithography steps. The use of hot wall-type RTP systems will be essential for tight control of electrical properties of devices with design rules beyond the 110 nm technology nodes.

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Keywords

1. Dynamic Random Access Memory (DRAM)

2. Implant Anneal

3. Rapid Thermal Processing (RTP)

4. Hot-Wall RTP System

5. Cold-Wall RTP System

6. Device Performance

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