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Implant Anneal Using a Single-Wafer Furnace and a Lamp-Based Rapid Thermal Annealing System

Woo Sik Yoo,[a,*,z] Takashi Fukada,[a,*] Tsuyoshi Setokubo,[b] Kazuo Aizawa,[b] Toshinori Ohsawa,[c] Nobuaki Takahashi,[d] and Keiichi Enjoji[d]

[a]*WaferMasters, Incorporated, San Jose, California 95112, USA*
[b]*NEC Hiroshima, Limited, Hiroshima, Japan 739-0198*
[c]*Tokyo Electron FE, Limited, Tokyo 183-8705, Japan*
[d]*Tokyo Electron Limited, Tokyo 107-8481, Japan*

Rapid thermal annealing (RTA) of various implant species ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$, and $^{75}As^+$) in 200 mm diam Si wafers was done using a single-wafer furnace (SWF) system and a lamp-based system under a N_2 ambient at atmospheric pressure. Sheet resistance and its uniformity were measured after annealing under various conditions. Equivalent or superior sheet resistance and uniformity were achieved in the SWF system compared to lamp-based RTA systems. The effect of annealing method, temperature, and time on dopant redistribution were investigated using secondary ion mass spectroscopy.
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Dopant diffusion and implant annealing have been done in both horizontal and vertical batch furnaces. Vertical batch furnaces have the comparative advantages of temperature uniformity, gravitational stress management, and cleanroom space usage over horizontal batch furnaces. It is strongly believed that single-wafer rapid thermal processing (RTP) is essential to reduce thermal exposure. The demand for RTP implant annealing has grown rapidly over the last ten years. In reality, both types of batch furnaces are able to meet the requirements for thermal processing applications, even for 0.18 μm technology[1] and beyond.

Typical RTP systems employ an array of tungsten halogen lamps to heat a wafer. The lamp-based RTP systems are frequently used in silicidation, rapid thermal oxidation (RTO), rapid thermal nitridation (RTN), and rapid thermal anneal (RTA), including implant annealing. The tungsten filaments used in the lamps are of small thermal mass enabling fast thermal response of the lamps as well as fast ramp up and ramp down of the wafer temperature. As device dimensions and junction depths decrease, RTP for implant annealing is believed to be the best solution. RTP manufacturers have begun competing for higher wafer temperature ramp rates and shorter process times. An RTP system for 200 mm wafers can use more than two hundred 500 W tungsten-halogen lamps.[2,3] Initial wafer temperature ramp up rate of ~250°C/s and process time approaches 0 s (called a spike anneal) are applied in annealing of implanted wafers.[2,3] Implanted wafers are often annealed above 1000°C for less than 60 s in RTP systems while they may be annealed at approximately 900°C for as much as 10-20 min in conventional batch furnaces.

The authors had fundamental questions regarding the effect of annealing temperature and annealing time on implant activation efficiency. Recently, a new RTP approach using a single-wafer-type furnace has been proposed. Its thermal characteristics and preliminary process results have been reported.[4-6] The single-wafer furnace (SWF) allows a short annealing time in a nearly isothermal furnace environment. In this paper, the authors investigated the effect of annealing temperature and annealing time on implant activation efficiency using both a SWF system and a conventional lamp-based RTP system.

Experimental.— 200 mm diam Si(100) wafers were implanted with four different species. Implant species, energies, and doses are as follows: $^{11}B^+$ 50 keV 1×10^{15} cm^{-2}; $^{49}BF_2^+$ 70 keV, 1×10^{15} cm^{-2}; $^{31}P^+$ 70 keV, 1×10^{15} cm^{-2}; and $^{75}As^+$ 70 keV, 1×10^{15} cm^{-2}.

Each group of wafers was divided into two groups and annealed in the SWF system and conventional lamp-based RTP system, respectively. Both systems were well maintained for mass production of devices and were calibrated prior to the experiment. The annealing temperature was varied from 900 to 1100°C in an N_2 atmosphere at atmospheric pressure for all four types of implanted wafers. Annealing time was varied from 10 to 150 s for the lamp-based RTP system. For a lamp-based RTP system, the process time is the soak time near the process temperature, regardless of overhead times (such as preheating, ramp-up, and ramp-down times). The preheating and ramp-up steps usually last for 20-30 s depending on annealing temperature. In the SWF system, the process time is the wafer residence time (from wafer-in to wafer-out) in a heated furnace (process chamber) and is equivalent to ramp up time plus soak time in the lamp-based RTP system. For the SWF system, 30 s was simply added to the process time used in the lamp-based RTP system to match the thermal history of wafers processed in the lamp-based RTP system. The annealing time for the SWF system was varied from 40 to 180 s. Details of the SWF system configurations and thermal characteristics are reported in previous publications.[4-6]

Sheet resistance (ρ_s) and its uniformity were measured using a four-point probe after annealing. Forty-nine points were measured with a 5 mm edge exclusion (no measurement points within 5 mm of the wafer edge). The effect of annealing on dopant redistribution was investigated using secondary ion mass spectroscopy (SIMS).

Results and Discussion

Figure 1 shows sheet resistance and sheet resistance uniformity plots for four different types of implanted wafers ($^{11}B^+$ 50 keV, 1×10^{15} cm^{-2}; $^{49}BF_2^+$ 70 keV, 1×10^{15} cm^{-2}; $^{31}P^+$ 70 keV, 1×10^{15} cm^{-2}; and $^{75}As^+$ 70 keV, 1×10^{15} cm^{-2}) as functions of process (annealing) temperature. Process (annealing) time was fixed at 40 s (from wafer-in to wafer-out) for the SWF system and 10 s (soak time at the process temperature) for the lamp-based RTP system. Both the SWF and lamp-based RTP annealing results are shown in the figure. All four types of implanted wafers were electrically activated for both wafer heating methods. Equivalent sheet resistance values were achieved in wafers annealed using both systems. Temperature sensitivity of sheet resistance and sheet resistance uniformity of $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers are higher than those of $^{31}P^+$ and $^{75}As^+$ implanted wafers in the temperature range of 900-1100°C.

For the SWF system, the sheet resistance uniformity in $^{49}BF_2^+$, $^{31}P^+$, and $^{75}As^+$ implanted wafers was below 1.0% (1 σ). The sheet resistance uniformity in $^{11}B^+$ implanted wafers was kept below 2.0% (1 σ). In the case of the lamp-based RTP system, only $^{31}P^+$ and $^{75}As^+$ implanted wafers showed sheet resistance uniformity be-

* Electrochemical Society Active Member.
[z] E-mail: woosik.yoo@wafermasters.com

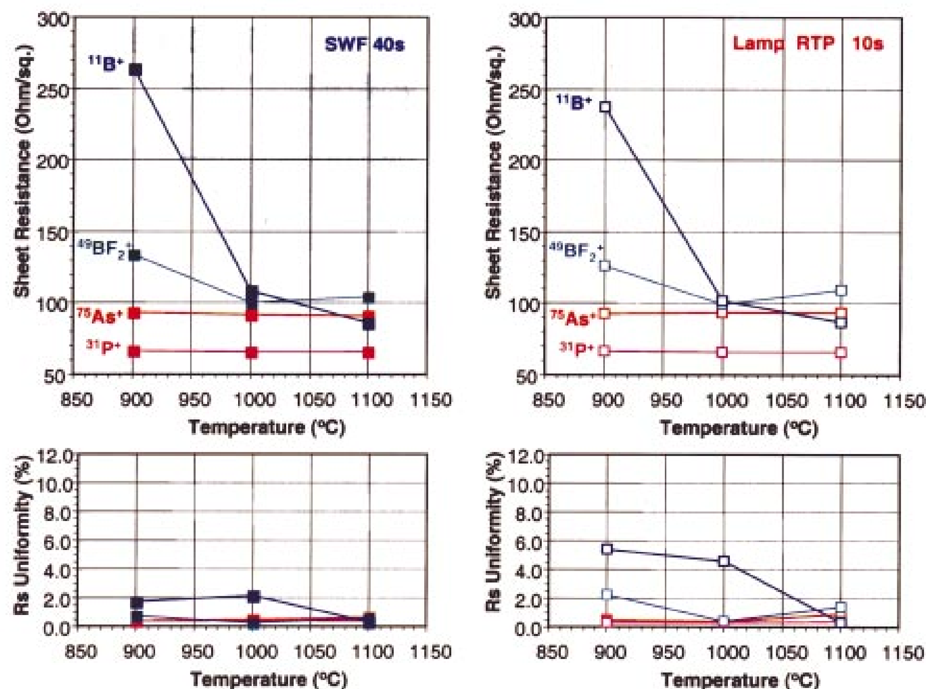

Figure 1. Sheet resistance and its uniformity of four different types of implanted wafers ($^{11}B^+$ 50 keV, 1×10^{15} cm^{-2}; $^{49}BF_2^+$ 70 keV, 1×10^{15} cm^{-2}; $^{31}P^+$ 70 keV, 1×10^{15} cm^{-2}; and $^{75}As^+$ 70 keV, 1×10^{15} cm^{-2}) as functions of annealing temperature.

low 1.0% (1 σ). In $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers, sheet resistance uniformity up to 5.4% (1 σ) was measured.

Sheet resistance and its uniformity for $^{49}BF_2^+$ (70 keV, 1×10^{15} cm^{-2}) implanted wafers are shown in Fig. 2 as a function of annealing temperature and time. As seen in the figure, the behavior of the sheet resistance and uniformity is very complex. In wafers annealed using the SWF system, sheet resistance decreases as the annealing time increases at 900°C. When the annealing temperature was raised to 1000°C and above, the sheet resistance increases with time. The sheet resistance uniformity also deteriorated significantly with increasing annealing time at 1100°C. A similar trend was observed using the lamp-based RTP system. The sheet resistance increase with increasing annealing temperature and time can be explained by the thermal diffusion of the implanted species in the wafer. As thermal diffusion progresses, the dopant concentration in the implanted region decreases resulting in increased sheet resistance. $^{31}P^+$ and $^{75}As^+$ implanted wafers showed similar trends while $^{11}B^+$ implanted wafers showed decreases in sheet resistance with increases in annealing temperature and time.

Response surfaces of sheet resistance and its uniformity for $^{49}BF_2^+$ (70 keV, 1×10^{15} cm^{-2}) implanted wafers are shown in Fig. 3. Wafers annealed in the SWF system showed lower sheet resistance and better uniformity over a wide range of annealing temperatures and times compared to those annealed in the lamp-based RTP system. Process windows are indicated in the figure. Sheet resistance value of <110 Ω/□ and uniformity of <0.5% (1 σ) were used as boundary conditions for process window determination. In general, longer annealing around 1000°C gives lower sheet resistance and better sheet resistance uniformity compared to short anneal times at higher temperatures regardless of the annealing system.

This result is contradictory to the basic concept of the spike anneal proposed by Jennings *et al.*[7] The objective of the spike anneal is to electrically activate implanted species with minimal thermal diffusion of implanted species by heating the wafer very rapidly and cooling the wafer as soon as the wafer reaches a target temperature. The spike anneal is often referred to as a 0 s process.[2,3,7] The target temperature is usually 50-200°C higher than normal RTP annealing temperature and conventional furnace annealing temperatures.

To understand the physics behind the implant anneal, we need to review how the implant anneal is done in conventional batch furnaces. It takes place over a temperature range of 800-950°C for 10-30 min. Very consistent sheet resistance and sheet resistance uniformities are achieved. However, the conventional batch furnace lacks lot size flexibility and requires longer cycle times. Three main reactions take place during implant anneal. They are (*i*) recrystallization (solid-phase regrowth) of the (amorphized) layer damaged during implantation, (*ii*) electrical activation of the implant species, and (*iii*) thermal diffusion of the implanted species. Full recrystallization of the amorphized layer and full electrical activation of implant species without thermal diffusion would be ideal for the implant anneal. It is well known that the solid-phase regrowth occurs at temperatures as low as 450°C. Solid-phase regrowth rates of silicon (100) at 600 and 800°C are approximately 1 and 500 nm/s, respectively.[8] In order to take place, electrical activation and dopant diffusion require higher thermal energy than solid-phase regrowth. Two well known facts are (*i*) the diffusivity of atoms in Si increases exponentially as annealing temperature increases and (*ii*) the increase in junction depth x_j is proportional to the square root of annealing time in the case of an infinite source on the surface.[9]

The diffusivity determined experimentally over a range of diffusion temperature is often expressed as

$$D = D_0 \exp\left(-\frac{E}{kT}\right) \quad [1]$$

where D_0 is the frequency factor in centimeters squared per second, E is the activation energy in electronvolts, T is temperature in kelvin, and k is the Boltzmann constant. In the case of a finite volume of material in which the impurity gradient decreases with increasing

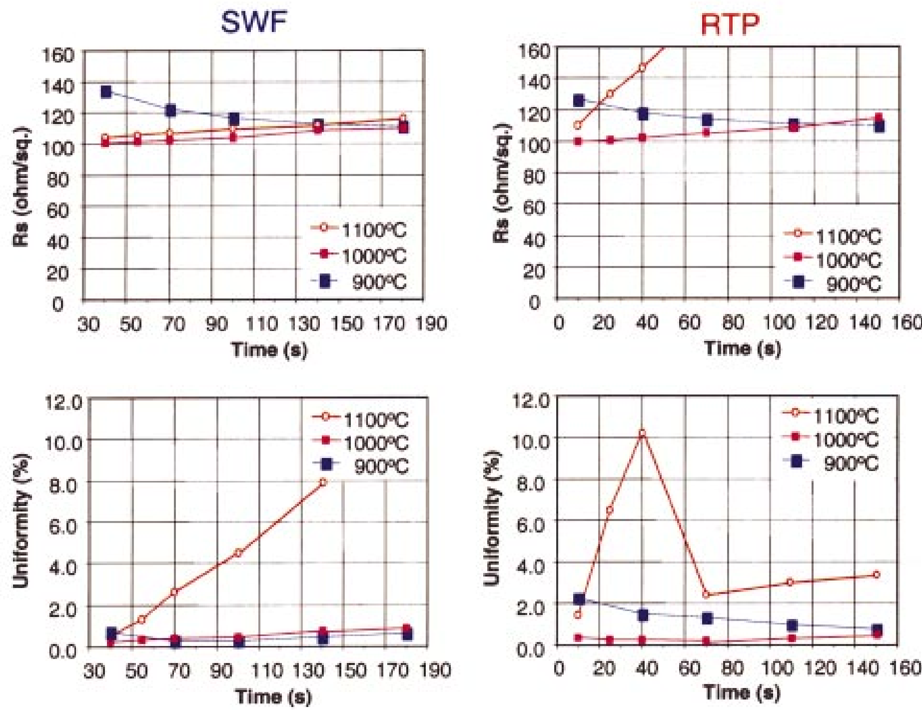

Figure 2. Sheet resistance and sheet resistance uniformity of $^{49}BF_2^+$ (70 keV, 1×10^{15} cm^{-2}) implanted wafers after annealing.

time, impurity concentration also changes with time. Diffusion behaviors can be understood by solving Frick's equation.[9]

In the case of diffusion from an infinite source on the surface, impurity concentration can be expressed as

$$N(x,t) = N_0\left[1 - \mathrm{erf}\left(\frac{x}{2\sqrt{Dt}}\right)\right] \quad [2]$$

where erf is the error function. If there is a background concentration N_1 of a different species of the opposite type, a junction will occur when

$$N_0\left[1 - \mathrm{erf}\left(\frac{x}{2\sqrt{Dt}}\right)\right] = N_1 \quad [3]$$

The junction depth x_j is given by

$$x_j = 2\sqrt{Dt}\,\mathrm{erf}^{-1}\left(1 - \frac{N_1}{N_0}\right) \quad [4]$$

which can be rewritten as

$$x_j = A\sqrt{t} \quad [5]$$

where A is a constant given by $A = 2[\mathrm{erf}^{-1}(1 - N_1/N_0)]\sqrt{D}$. Thus the junction depth x_j increases as the square root of the diffusion time. In the limited-source case, such as ion implanted wafers, the surface concentration decreases linearly with $\sqrt{t}$. The junction depth varies in a more complex manner and can be expressed as

$$x_j = \left[4Dt\ \log\left(\frac{S}{N_B\sqrt{\pi Dt}}\right)\right]^{1/2} = 2\sqrt{Dt}\left[\log\left(\frac{S}{N_B\sqrt{\pi Dt}}\right)\right]^{1/2} \quad [6]$$

where S is the total number of impurities and N_B is the background concentration. $\sqrt{Dt}$ is referred as the diffusion length. The junction depth x_j initially increases as the square root of diffusion time, then it slows as the maximum impurity concentration decreases with time.

Figure 4 shows SIMS depth profiles of implanted [$^{49}BF_2^+$ (70 keV, 1×10^{15} cm^{-2})] and annealed wafers in both SWF and RTP systems. At a given annealing temperature, dopant depth profiles are almost identical regardless of annealing method (or equipment) as long as the sheet resistance values are equivalent. Both high-temperature anneals and long-time anneals enhance dopant diffusion. The wafer annealed at 1100°C for 40 s (in SWF) and the wafer annealed at 1000°C for 100 s resulted in almost identical sheet resistance values. However, the wafer annealed at 1000°C for 100 s (in SWF) shows less boron diffusion compared to the wafer annealed at 1100°C for 40 s. By contrast, the wafer annealed at 1100°C for 10 s in the lamp-based RTP system resulted in almost identical boron depth profiles as both the wafer annealed at 1000°C for 70 s in the lamp-based RTP system and the wafer annealed at 1000°C for 100 s in the SWF system. Among them, the wafer annealed at 1100°C for 10s in the lamp-based RTP system showed the highest sheet resistance value (109.80 Ω/□). Oscillation of boron concentration was consistently seen in the lamp-based RTP system at 1100°C for all exposures in excess of 25 s. Similar trends on electrical activation and dopant activation were observed in other implant species. This result poses a question regarding the validity of the spike anneal.

To achieve maximum electrical activation with minimum dopant diffusion, the implant anneal must be performed at optimum (not necessarily higher) temperatures for reasonable times. This process

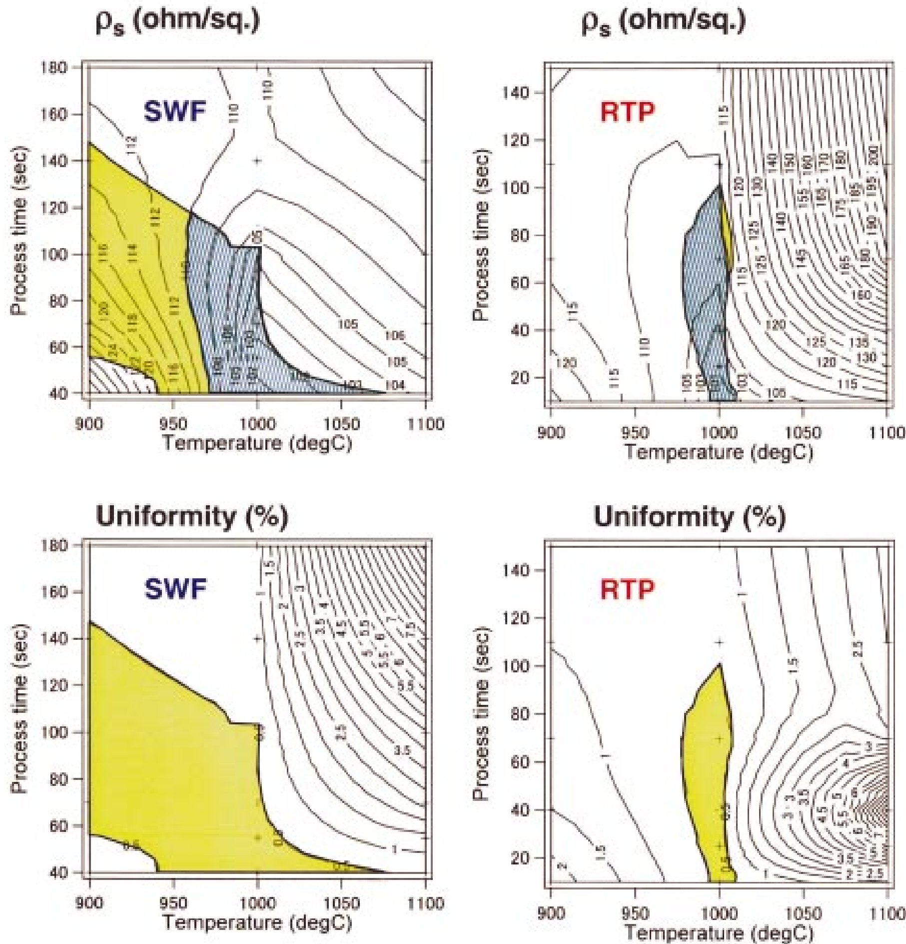

Figure 3. Process window determined on response surface of sheet resistance and sheet resistance uniformity of $^{49}BF_2^+$ (70 keV, 1×10^{15} cm^{-2}) implanted wafers after annealing. (Boundary conditions: sheet resistance $<110\ \Omega/\square$ and sheet resistance uniformity $<0.5\%$ in 1 σ.)

has been used in furnaces for many years. If this furnace-oriented implant anneal process is implemented in a single-wafer RTP system, productivity of the system will decrease significantly. Many RTP system providers and device manufacturers focus on development of a short-time anneal at higher temperatures varying wafer temperature ramp-up/down rates such as the spike anneal. Thermal physics and process results in this study suggest that the furnace-oriented implant anneal provides wider process windows for implant annealing than the state-of-the-art spike anneal.

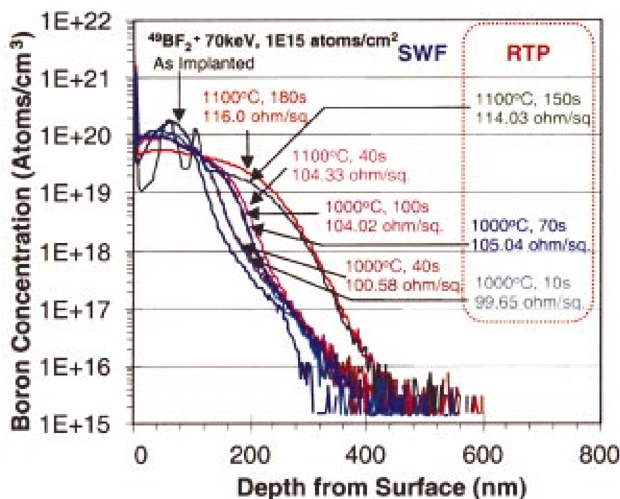

Figure 4. SIMS depth profiles of implanted [$^{49}BF_2^+$ (70 keV, 1×10^{15} cm^{-2})] and annealed wafers processed in SWF and RTP systems.

At a given implant uniformity, the sheet resistance uniformity is strongly dependant upon the uniformity and stability of the thermal environment in which wafers are processed. Lamp-based RTP systems operate as a cold-wall-type system and lack thermal stability. Wafers are always processed in thermal transient conditions. As the process time shortens, the transient effect is pronounced. In hot-wall-type systems such as furnace and SWF systems, wafers are processed near thermal equilibrium. Thus hot-wall-type systems generally provide superior process uniformity without sophisticated temperature control mechanisms. Based on the experimental results in this study, we can conclude that equivalent or superior sheet resistance and its uniformity were achieved in the SWF system compared to the lamp-based RTP system. The high-temperature spike anneal process can be replaced by a more reasonable annealing process (60-180 s annealing) using either hot-wall-type SWF system or the lamp-based RTP systems. In terms of process simplicity and energy efficiency, the SWF system is superior to the lamp-based RTP systems. Energy efficiency comparisons are discussed in detail in previous papers.[4-6] SWF systems also offer lot size flexibility and equivalent or better productivity compared to lamp-based RTP systems.[4-6] Rapid thermal annealing of implanted wafers with different implant energies and dose conditions will be performed to further investigate the validity of the spike anneal for shallow junction implant annealing.

Conclusions

RTA of various implant species ($^{11}B^+$, $^{49}BF_2^+$, $^{31}P^+$, and $^{75}As^+$) in 200 mm diam Si wafers was done using a resistively heated SWF system and lamp-based conventional RTP system under a N_2 ambient at atmospheric pressure. Sheet resistance and sheet resistance uniformity were measured after annealing under various conditions. Single variable test results and surface responses of sheet resistance and its uniformity were plotted as functions of annealing temperature and time. Lower sheet resistance and superior sheet resistance uniformity were achieved compared to lamp-based conventional RTA systems. The high temperature spike anneal process can be replaced by a more reasonable annealing process (60-180 s annealing) using either the hot-wall-type SWF systems or lamp-based RTP systems. Relatively longer annealing times at lower temperatures are favorable for efficient electrical activation with minimum dopant redistribution. The validity of the spike anneal is discussed based on experimental results as well as electrical activation and dopant diffusion mechanisms in implanted Si wafers. The effect of the annealing method, temperature, and time on dopant redistribution were investigated using SIMS.

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