RAPID THERMAL IMPLANT ANNEALING USING COLD WALL AND HOT WALL SYSTEMS

Woo Sik Yoo[1*], Takashi Fukada[1], Tsuyoshi Setokubo[2], Kazuo Aizawa[2], Jiro Yamamoto[2] and Ryuichi Komatsubara[3]

[1] WaferMasters, Inc.
246 East Gish Road, San Jose, CA 95112 U.S.A.
[2] NEC Hiroshima Limited,
7-10 Yoshikawa Kogyodanchi, Higashi Hiroshima, Hiroshima, 739-0198, Japan
[3]Tokyo Electron Ltd
3-6 Akasaka 5-chome, Minato-ku, Tokyo, 107-8481, Japan

Rapid thermal annealing (RTA) of $^{75}As^+$, $^{31}P^+$, $^{11}B^+$ and $^{49}BF_2^+$ implanted Si wafers (200 mm in diameter) was done using a lamp-based RTA ("cold wall") system and a single wafer rapid thermal furnace (SRTF: "hot wall") system under 1 atm N_2 atmosphere to investigate electrical activation and dopant diffusion phenomena. The implant energy and dose were varied in the range of 3 keV~70 keV and 1×10^{15}~1×10^{16} cm^{-2}, respectively. Average sheet resistance and uniformity of implanted wafers were measured after annealing. Change in depth profiles of implant species after annealing was investigated using the secondary ion mass spectroscopy (SIMS). Equivalent sheet resistance and uniformity are achieved after annealing regardless of annealing method. Significant difference in dopant depth profiles near the surface was observed between wafers annealed in lamp-based RTA and SRTF systems.

INTRODUCTION

Rapid thermal annealing (RTA) has became the preferred implant annealing method. A very short time annealing at higher temperature with a very fast ramp up/down rate ("spike anneal") has been introduced as an effective implant annealing method to electrically activate implant species with the least amount of diffusion during the annealing process [1-2]. The process window of the spike anneal is very narrow because it strongly relies on accuracy and repeatability of temperature measurement/control in a wide temperature range (room temperature ~1150°C) during a very short period of annealing time (<1s). For the successful formation of shallow junctions in production environment, a wide annealing process window for a low sheet resistance and abrupt dopant profiles are required. Fundamental understanding of damage recovery, electrical activation and dopant diffusion mechanisms during implant anneal is necessary.

In this study, RTA of $^{75}As^+$, $^{31}P^+$, $^{11}B^+$ and $^{49}BF_2^+$ implanted Si wafers (200 mm in diameter) was done using a lamp-based RTA ("cold wall") system and a single wafer rapid thermal furnace (SRTF: "hot wall") system at 1 atm N_2 atmosphere to investigate electrical activation and dopant diffusion phenomena in the "cold wall" and "hot wall" type systems. The similarity and difference in electrical activation and dopant profiles of wafers after annealing in the "cold wall" and "hot wall" type systems were investigated. Electrical activation and dopant redistribution behavior during annealing and impact of dopant profile on sheet resistance measurement are discussed based on experimental results.

* E-mail: woosik.yoo@wafermasters.com Phone: +1-408-451-0856 Fax: +1-408-451-9729

EXPERIMENTAL

A. Cold Wall System (Lamp-based RTA System)

A lamp-based RTA system is used as the "cold wall" system (Fig.1 (a)). The cold wall system used in this study employs banks of linear tungsten halogen lamp arrays and illuminates a Si wafer from both top and bottom arrays through the quartz process tube. The Si wafer is heated by absorbing photons emitted from lamps and transmitted through the cold quartz process tube. The wafer temperature is higher than surrounding quartz walls during annealing. Wafer temperatures are measured using a pyrometer through the quartz tube. A multiple zone power control method is used to adjust temperature uniformity on a Si wafer. Wafer temperature ramp up rate, soak time and ramp down rate are programmable.

B. Hot Wall System (SRTF System)

A dual chamber SRTF system with a vacuum loadlock was used as the "hot wall" system (Fig.1 (b)) in this study. The process tube is made of clear quartz and has three quartz standoffs. The process tube is heated to a desired process temperature and the temperature is kept constant. A Si wafer is heated by surrounding hot walls during annealing. The process tube uses no moving parts for design simplicity and system reliability. The wafer is placed on the quartz standoffs (8~9 mm tall) in the middle of quartz process tube. The separation between the wafer and the quartz walls is kept at ~10mm for both upward and downward directions. The quartz process tube is located in a SiC cavity which acts as a heat distributor to create an isothermal process environment. The SiC cavity is surrounded by a three zone heater assembly. The temperature of the SiC cavity is monitored and controlled at a predetermined process temperature by three embedded R-type thermocouples and the three zone heater assembly. Detailed configuration, thermal characteristics and process performance of the system have been reported elsewhere [3].

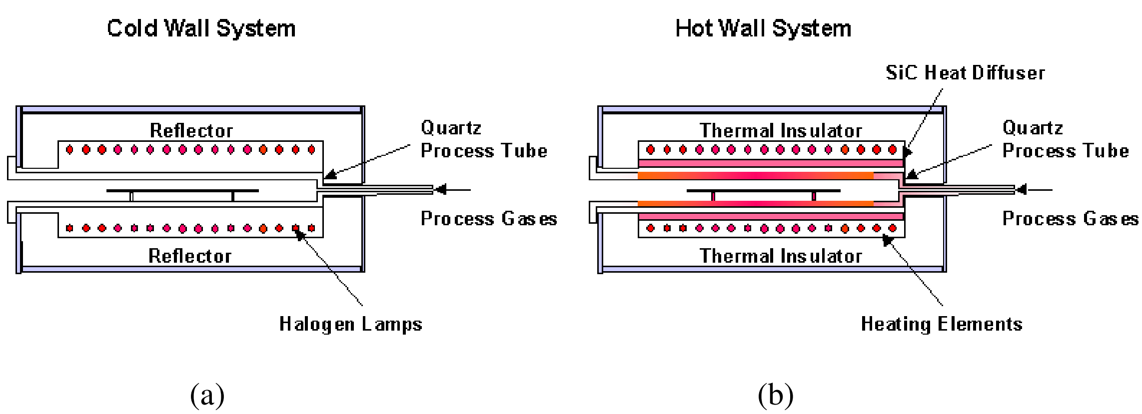

Fig. 1. Schematic illustration of wafer heating mechanisms in "cold wall" (a) and "hot wall" (b) systems.

C. Implant Anneal

Implant wafers were annealed using the lamp-based RTA system and SRTF system in a mass production environment. The implant energy and dose were varied in the range of 3 keV~70 keV and 1×10^{15}~1×10^{16} cm^{-2}, respectively. Two hundred millimeter (200 mm) diameter Si wafers implanted with various species were annealed using the lamp-based RTA system and SRTF system under 1 atm N_2 atmosphere to compare the resulting average sheet resistance and its uniformity after annealing. The annealing temperature was varied between 900°C and 1100°C. Figure 2 shows typical wafer temperature profiles during the annealing process at 1000°C. Process time (wafer residence time in the furnace) for the SRTF system in the temperature range of 900°C~1100°C can be easily estimated by simply adding 30s to the "soak time" in the lamp-based RTA system because it is approximately equal to "ramp up time" plus "soak time" in the lamp-based RTA system. Average sheet resistance measurement after implant anneal at 1000°C using the SRTF system and lamp-based RTA system indicated that the estimated process (residence) time for the SRTF system (30s addition to the "soak time" in the lamp-based RTA system) gives equivalent average sheet resistance after annealing. The annealing (soak) time for the lamp-based RTA system was varied between 10s and 150s. The annealing (residence) time for the SRTF system was varied between 40s and 180s.

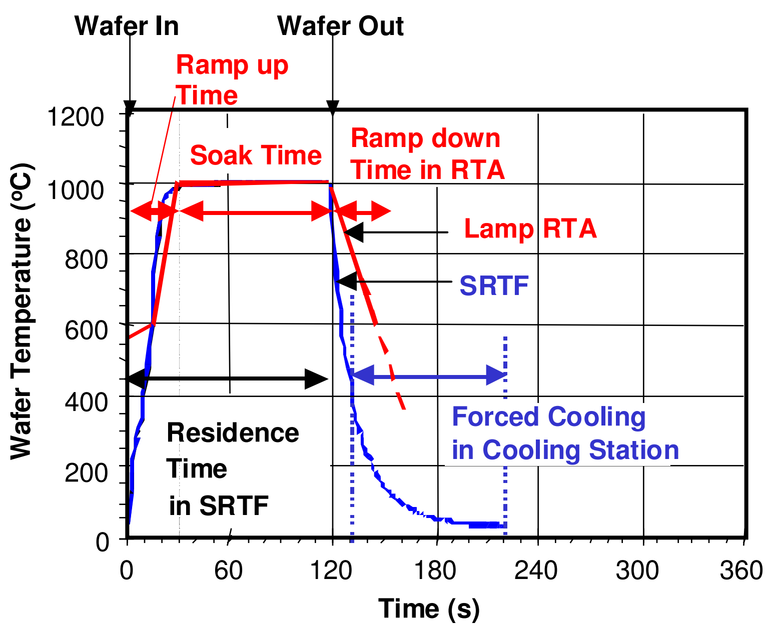

Fig. 2. Typical wafer temperature profiles during 90s (soak time) process in lamp-based RTA system and 120s process (residence time) in SRTF system.

D. Characterization

The sheet resistances of annealed wafers were measured at 49 points using a four-point probe. Five millimeter (5 mm) edge exclusion was used during the sheet resistance measurement. Surface response of average sheet resistance and its uniformity were used for process window determination. Dopant depth profiles were also measured before and after annealing using secondary ion mass spectroscopy (SIMS) to investigate dopant diffusion during annealing.

RESULTS AND DISCUSSION

Temperature sensitivity of average sheet resistance and uniformity of four different types of implanted wafers ($^{75}As^+$ 70 keV, $1x10^{15}$ cm^{-2}, $^{31}P^+$ 70 keV, $1x10^{15}$ cm^{-2}, $^{11}B^+$ 50 keV, $1x10^{15}$ cm^{-2} and $^{49}BF_2^+$ 70 keV, $1x10^{15}$ cm^{-2}) were plotted in Fig. 3. The soak time for the lamp-based RTA system was fixed at 10s. The residence time for the SRTF system was fixed at 40s (30s addition to the soak time for the lamp-based RTA system). All implanted wafers were electrically well activated above 1000°C regardless of wafer heating method (either lamp-based RTA system or SRTF system). The average sheet resistance values are almost identical between wafers annealed using different systems. A higher temperature sensitivity of sheet resistance was observed in p-type dopant ($^{11}B^+$ and $^{49}BF_2^+$) implanted wafers compared to ones implanted with n-type dopants ($^{75}As^+$ and $^{31}P^+$). However, superior sheet resistance uniformity was obtained in implanted wafers annealed using the SRTF system.

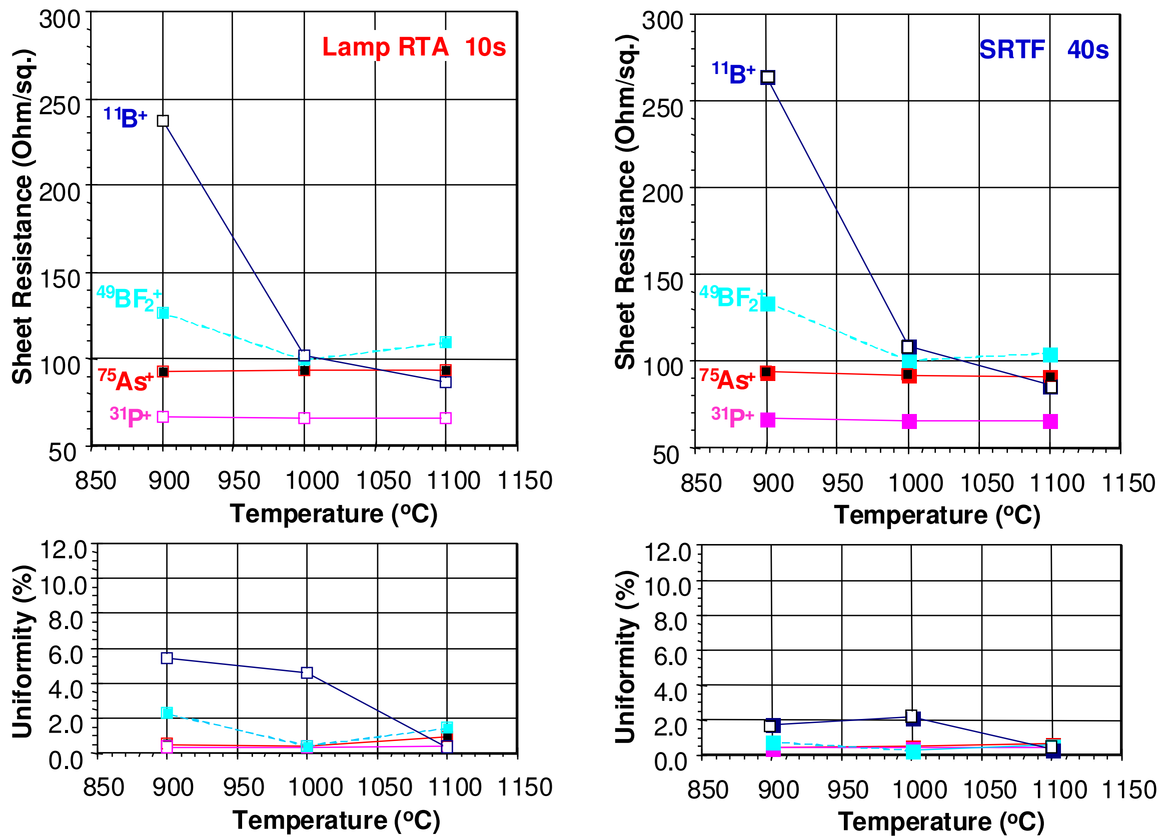

Fig. 3. Average sheet resistance and its uniformity (1σ) on implanted wafers after annealing in lamp-based RTA and SRTF systems.

Surface response of average sheet resistance of $^{75}As^+$ implanted wafers (70 keV, $1x10^{15}$ cm^{-2}) after annealing using the lamp-based RTA system and SRTF system are plotted in Fig. 4. A contour line of average sheet resistance uniformity at 0.5% (1σ) is also plotted on the surface response of average sheet resistance. The shaded regions in Fig. 4 represents process windows for boundary conditions of an average sheet resistance ρ_s<92(Ω/sq.) and its uniformity <0.5%(1σ).

In the lamp-based RTA system, the average sheet resistance value decreases as annealing temperature and annealing time increase in the temperature range of 900°C~1000°C. A reverse trend was observed in the temperature range of 1000°C~1100°C. The average sheet resistance value increases as annealing temperature and annealing time increase in the temperature range of 1000°C ~1100°C.

Similar trends in the average sheet resistance were observed in $^{75}As^{+}$ implanted wafers annealed using the SRTF system. Additionally, a lower average sheet resistance was obtained in wafers annealed using the SRTF system in the temperature range of 900°C~1100°C. The sheet resistance uniformity of wafers annealed using the SRTF system was always better. As a results of the lower sheet resistance and better sheet resistance uniformity, the process window for the SRTF system was found to be almost 4 times larger than that for the lamp-based RTP system.

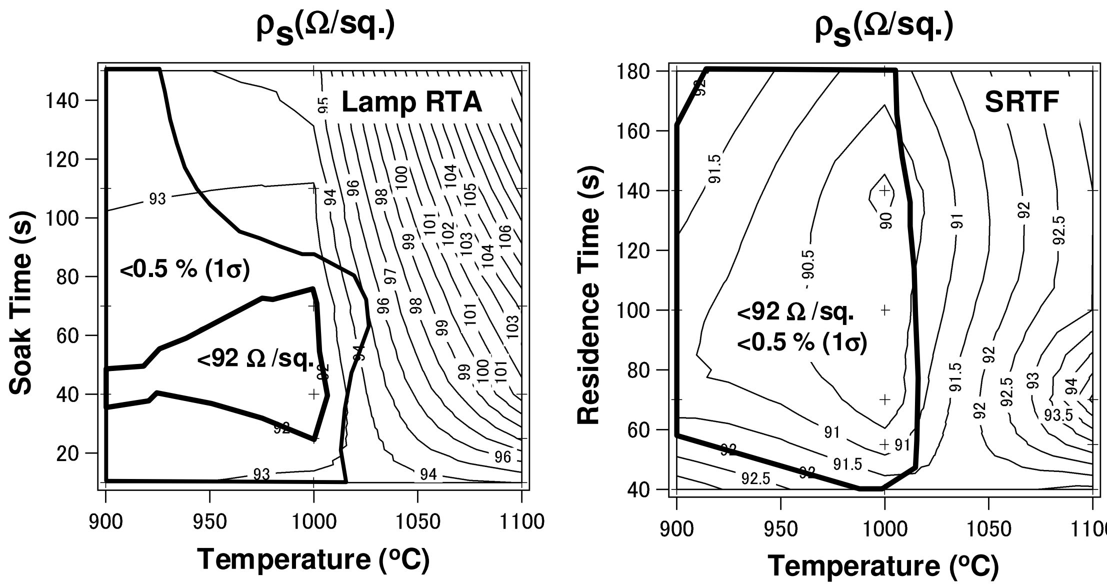

Fig. 4. Surface response of sheet resistance of $^{75}As^{+}$ implanted wafers after annealing using lamp-based RTA and SRTF systems. ($^{75}As^{+}$ 70keV, $1x10^{15}$ cm^{-2})

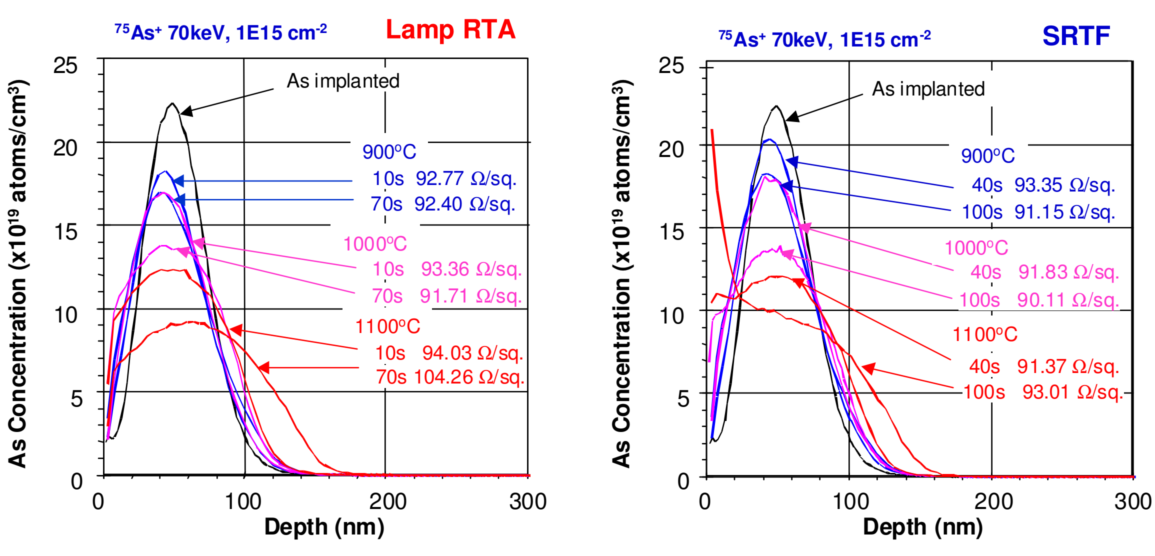

Fig. 5. Linear SIMS depth profiles of $^{75}As^{+}$ implanted wafers after annealing using lamp-based RTA and SRTF systems. ($^{75}As^{+}$ 70keV, $1x10^{15}$ cm^{-2})

SIMS depth profiles of $^{75}As^+$ implanted wafers (70keV, 1x10^{15} cm^{-2}) after annealing using the lamp-based RTA system and SRTF system are plotted in Fig. 5 in linear scale for easy comparison of dopant redistribution after annealing. The average sheet resistance values are indicated along with individual dopant depth profile. As seen in the figures, dopant diffusion increases with temperature and time. The average sheet resistance decreases as dopants electrically activate during RTA. Sufficient electrical activation has been observed in wafers annealed at 900°C regardless of the annealing system. Wafers annealed for 70s always showed lower average sheet resistance values compared to wafers annealed for 10s at 900°C and 1000°C. Conversely, the wafer annealed for 70s showed higher average sheet resistance value compared to the wafer annealed for 10s at 1100°C using the lamp-based RTP system. The increase in sheet resistance is due to resistivity increase in the implanted region by an excessive dopant diffusion. Similar trends were observed in wafers annealed using the SRTF system.

In the initial stage of annealing, dopant nearly symmetrically diffuses in both surface and bulk directions and maximum dopant concentration gradually decreases with time. As annealing proceeds, the dopant profile becomes asymmetrical. The dopant concentration near the surface increases initially and decreases due to the one-way diffusion into bulk with increase of annealing time. In wafers annealed at 1100°C using the SRTF system, maximum dopant concentration was observed at the surface of wafer. The dopant concentration at the surface was always higher in wafers annealed using the SRTF system compared to wafers annealed using the lamp-based RTA system.

The authors believe that the difference in dopant depth profiles between wafers annealed using the lamp-based RTP system and the SRTF system is caused by the difference in wafer heating mechanism. The lamp-based RTP system and SRTF system can be classified as "cold wall" system and "hot wall" systems, respectively. The lamp-based RTP system uses an internal heating mechanism whereas the SRTF system uses an external heating mechanism. At a given wafer temperature, the SRTF system always gives higher surface temperature. The higher surface temperature makes dopant diffusion to the surface easier. The dopant "pile up" near the surface or SiO_2/Si interface region was reported in previous implant anneal studies using conventional furnace technology [4-5]. The dopant pile up phenomena was also observed in all four types ($^{75}As^+$, $^{31}P^+$, $^{11}B^+$ and $^{49}BF_2^+$) of implanted wafers annealed using the SRTF system, regardless of implant energy and dose. We can conclude that the dopant pile-up is a common phenomena observed in implanted wafers using the "hot wall" systems. From the device fabrication point of view, higher dopant concentration at the wafer surface is desirable to reduce contact resistance. Single wafer type furnaces such as the SRTF system, can be useful for implant activation with contact resistance reduction.

CONCLUSIONS

Rapid thermal annealing (RTA) of $^{75}As^+$, $^{31}P^+$, $^{11}B^+$ and $^{49}BF_2^+$ implanted Si wafer (200 mm in diameter) was accomplished using a lamp-based RTA ("cold wall") system and a single wafer rapid thermal furnace (SRTF: "hot wall") system at 1 atm N_2 atmosphere. The implant energy and dose were varied in the range of 3 keV~70 keV and 1x10^{15}~1x10^{16} cm^{-2}, respectively. Average sheet resistance and uniformity of implanted wafers were measured after annealing. Change in depth profiles of implant species after annealing was investigated using secondary ion mass spectroscopy (SIMS). Electrical activation and dopant diffusion phenomena were compared after annealing using the lamp-based RTA and SRTF systems. Equivalent sheet resistance and uniformity are achieved after annealing regardless of the annealing method. Significant difference in dopant depth profiles near the surface was observed between wafers annealed in lamp-based RTA and SRTF systems. The dopant pile up near the surface was only observed in implanted wafers annealed using the SRTF system. It was observed in all four types ($^{75}As^+$, $^{31}P^+$, $^{11}B^+$ and $^{49}BF_2^+$) of implanted wafers annealed using the SRTF system. The dopant pile up mechanism was explained by a diffusion model and the difference in wafer heating mechanisms between the "cold wall" and "hot wall" systems.

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